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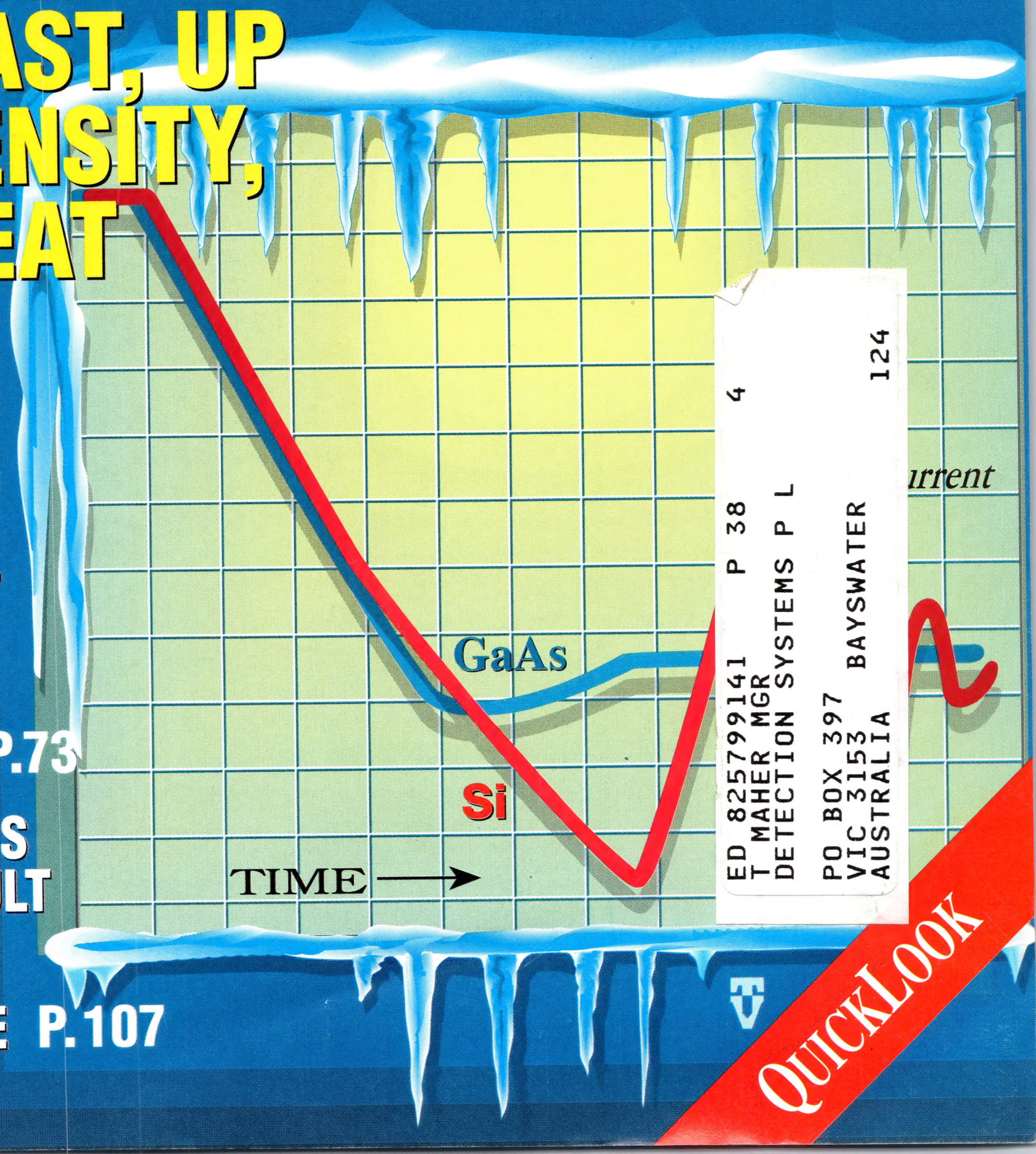

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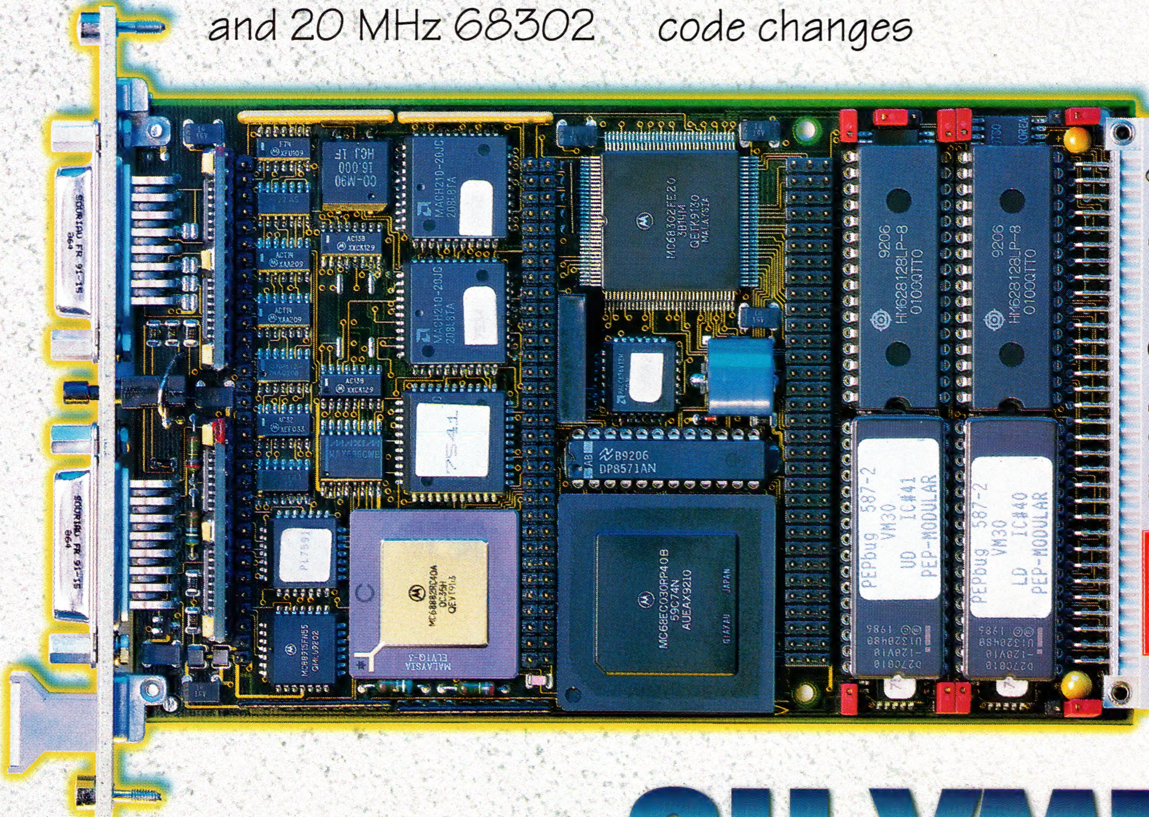
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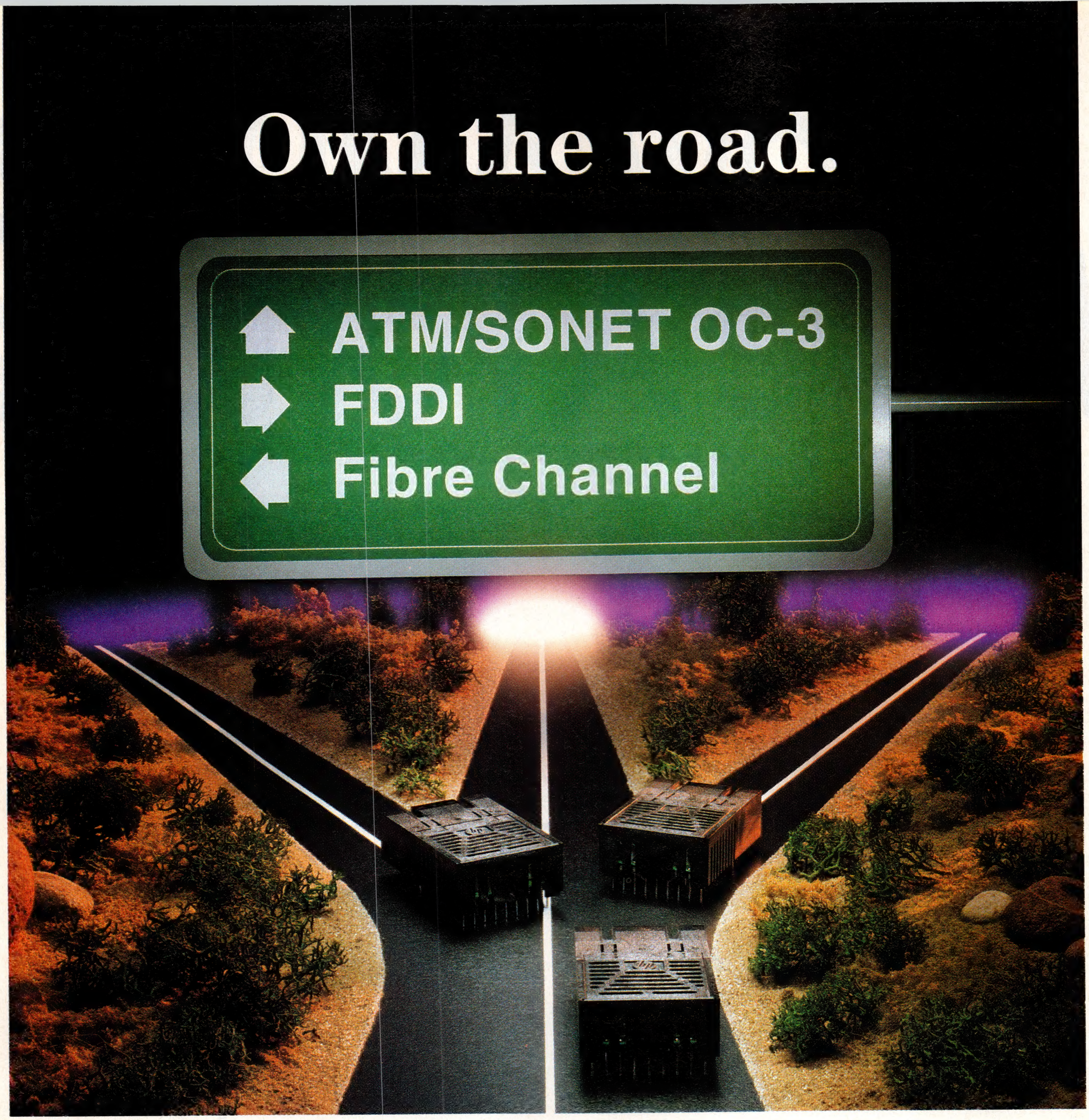

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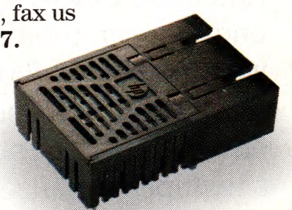

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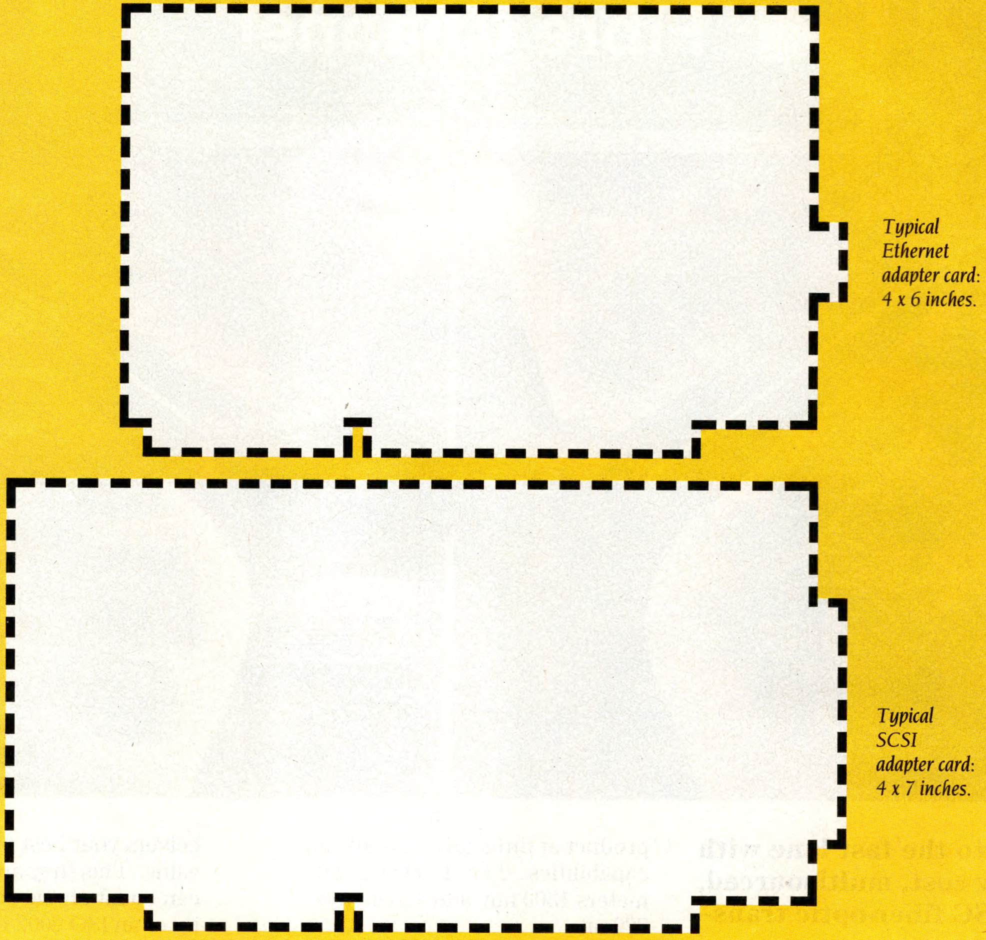

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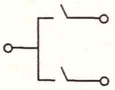
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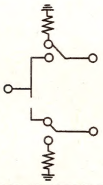
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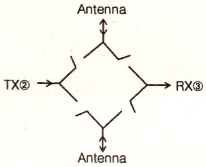

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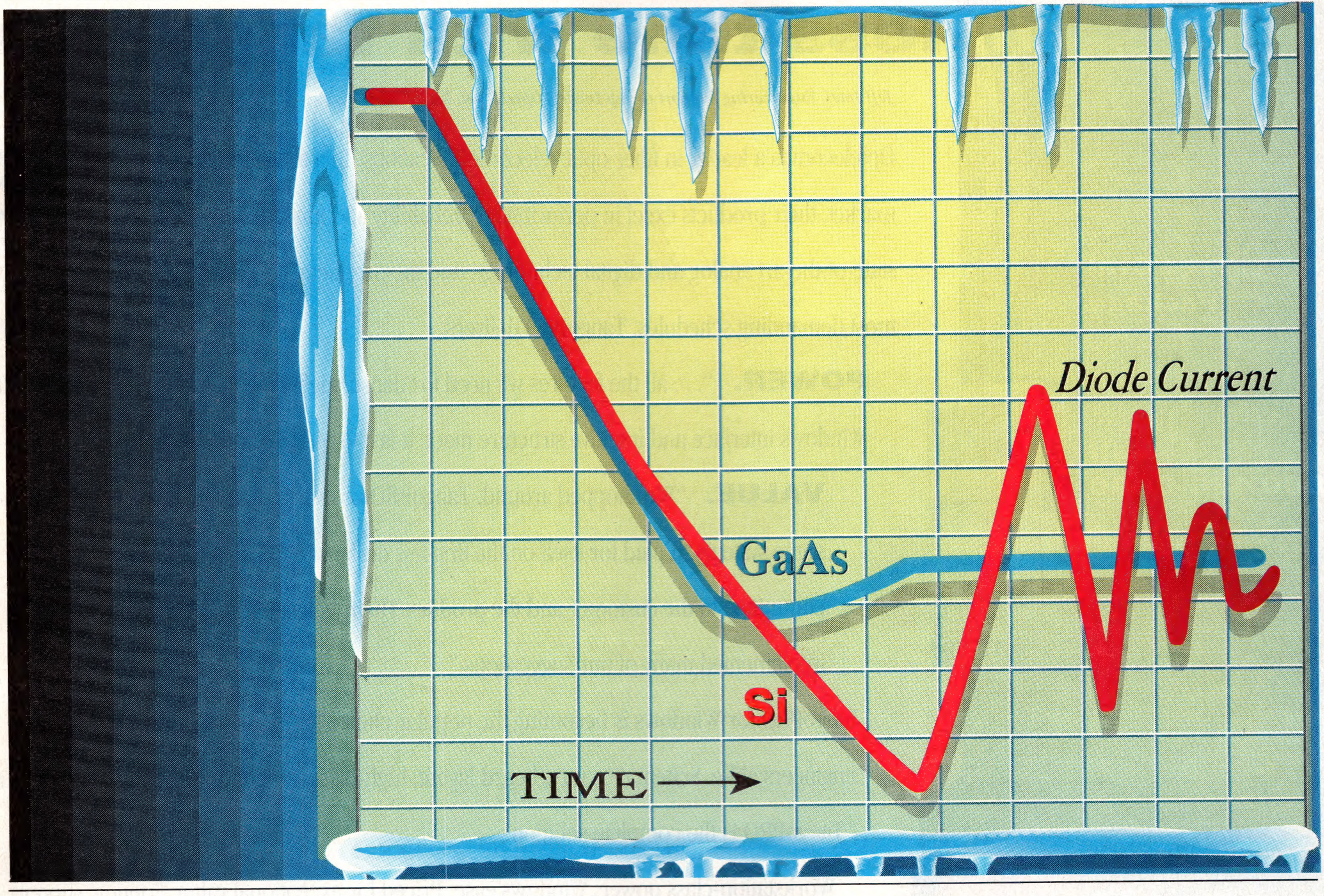

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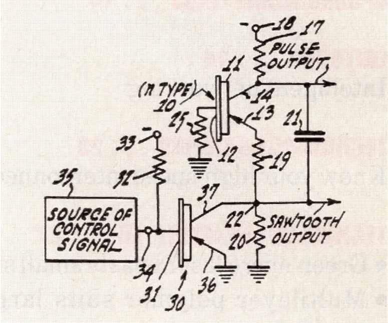
ELECTRONIC DESIGN 40 YEARS AGO

Patents: Frequency Controlled Oscillator System ...Patent No. 2,663,800. G.B. Herzog. (Assigned to Radio Corp. of America)

A transistor has two regions of operation, one of low conduction, which is a stable state, and the other of high conduction, which is an unstable state. An oscillator system that makes use of this characteristic has been devised by George C. Sziklai and is used in the circuit illustrations of this patent. The transistor control circuit shown controls the frequency of such an oscillator. The oscillator system described has particular applicability for control of the generation of a saw tooth wave for television receivers.

The oscillator circuit includes the capacitor 21, which is charged through resistors 20 and 17 from a current source or battery, the negative terminal being connected at 18 and the positive terminal grounded. An n type transistor (11) may serve as a discharge circuit. Its collector 14 and emitter 13 with a resistor (19) are connected in parallel with condenser 21. The capacitor begins to charge and the current flow through resistors 20 and 17 establishes a relatively low potential with respect to ground at point 22 and a relatively high potential with respect to the source potential at collector 14, so that the potential across the emitter-collector electrodes is within the low conduction stable state of the transistor. As the charge on the condenser increases, the current flow decreases which raises the potential at point 22 and lowers that at 14 until the potential across electrodes 13 and 14 reaches the value at which the transistor makes a sudden shift to its high conduction unstable state. The condenser then discharges to restore initial conditions, whereupon the cycle repeats.



A p-n-p type of transistor (30) controls the frequency of the oscillations by having its emitter 36 and collector 37 connected in parallel with the resistor 20. The impedance between these two transistor electrodes is controlled by the current supplied from a signal source (35). The required bias for the base electrode (31) is supplied by a resistor (32) and a current source at terminal 33. By changing the current from control signal source 35, the impedance between collector 37 and emitter 36 is changed, which in turn changes the impedance of the parallel circuit, including the resistor 20 and the rate of charging of capacitor 21. This action controls the frequency of the oscillator. The control transistor may have its collector-to-base circuit in parallel with the resistor as illustrated in other forms of the circuit. *(Electronic Design, August 1954, p. 73.)*

The author of this patent, Jerry Herzog, a 40-year veteran of the semiconductor industry, is now retired and resides in San Jose, Calif. He says he remembers this patent well, because it represented a significant development:

"This circuit was a key element in the first all-solid-state television set, which was built in 1952 at RCA's David Sarnoff Research Center. The point-contact transistor (Item 10) created a pulse output that drove the horizontal output transistors via a high-efficiency complementary-symmetry pulse amplifier. Because the experimental high-voltage power transistors of those days had so much storage delay, if the oscillator was merely locked to the horizontal sync pulse, the horizontal blanking bar appeared in the middle of the screen with half the picture on each side. This circuit was used to control the frequency via a phase-locked loop with the pnp junction transistor (Item 30) modulating the current flowing to the oscillator, thereby controlling its frequency and solving the problem."

Herzog worked on this circuit during his first year with RCA, and spent most of his career with the company. He later was Vice President at RCA Semiconductor's Solid-State Technology Center, Somerville, N.J. Herzog eventually joined Texas Instruments, and then migrated further west, into retirement. He now spends much time touring the U.S. in his motor home.—SS

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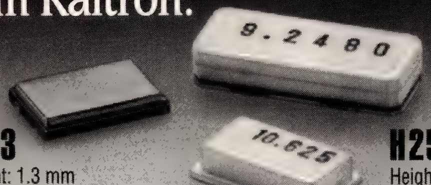

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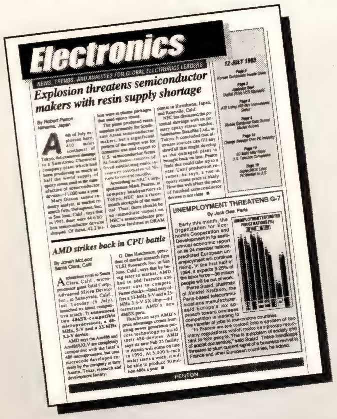

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Advertising Production:
(201) 393-6093 or Fax (201) 393-0410

Production Manager: Mike McCabe
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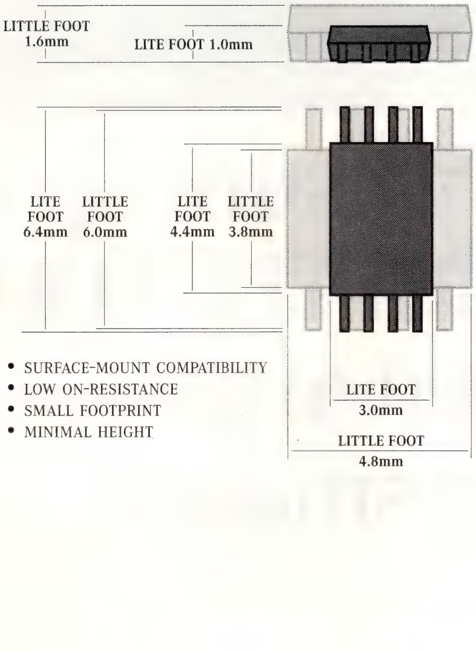

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Si6433DQ	Single P-Ch	-12	75	3.5
Si6447DQ	Single P-Ch	-20	100	3.0
Si6953DQ	Dual P-Ch	-20	200	1.7
Si6542DQ	Complementary N-Ch P-Ch	 20 -20	 100 200	 2.5 1.7

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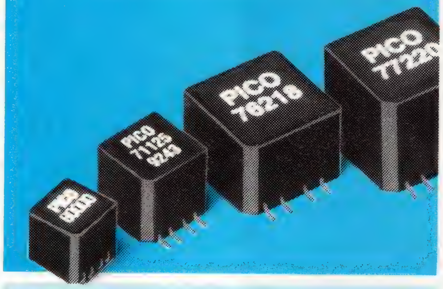

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UPCOMING MEETINGS

AUGUST

IEEE Magnetic Recording Conference (TMRC '94), Aug. 16-20. University of California, La Jolla, CA. Contact Roger F. Hoyt, IBM Almaden Research Center, 650 Harry Rd., K01/803, San Jose, CA 95120-6099; (408) 927-2118; fax (408) 927-3204.

IEEE International Symposium on Electromagnetic Compatibility, Aug. 22-26. Palmer House Hotel, Chicago, IL. Contact H. R. Hofmann, 1210 Lawn Meadow Ln., Naperville, IL 60540; (708) 979-3627; fax (708) 979-5755.

Conference on Lasers & Electro-Optics, Europe & The 5th European Quantum Electronics Convention (CLEO EUROPE/EQEC), Aug. 28-Sept. 2. RAI Congress Centre, Amsterdam, The Netherlands. Contact Susan Evans, IEEE/LEOS, 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3896; fax (908) 562-1571.

SEPTEMBER

IEEE International Symposium on Compound Semiconductors, Sept. 18-22. Del Coronado Hotel, San Diego, CA. Contact James Harbison, Bellcore, 331 Newman Springs Rd., Room 3X-211, Red Bank, NJ 07701; (908) 758-3386; fax (908) 758-4372.

14th IEEE International Semiconductor Laser Conference, Sept. 19-23. Hyatt Regency Maui, Maui, HI. Contact Samantha H. Phillips, IEEE/LEOS, 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3894; fax (908) 562-1571; E-mail: s.phillips@ieee.org.

ASIC Conference and Exhibit (ASIC '94), Sept. 19-23. Rochester Riverside Convention Center, Rochester, NY. Contact Paul P. K. Lee, Eastman Kodak Co., Rochester, NY 14650-2008; (716) 477-2869; fax (716) 477-4947.

AUTOTESTCON '94, Sept. 20-22. Disneyland Hotel, Anaheim, CA. Contact Robert Rassa, ManTech International, 150 S. Los Robles Ave., Suite 350, Pasadena, CA 91101; (818) 577-7100; fax (818) 577-7102.

Embedded Systems Conference, Sept. 20-23. Santa Clara Convention Center, Santa Clara, CA. Contact (415) 905-2354 for more information.

Canadian Conference on Electrical and Computer Engineering, Sept. 25-28. World Trade & Convention Centre, Halifax, Nova Scotia. Contact C. Baird, Dept. of Electrical Engineering, Technical University of Nova Scotia, P. O. Box 1000, Halifax, Nova Scotia, B3J 2X4 Canada; (902) 420-7717; fax (902) 422-7535.

Information Superhighway Summit/San Jose, Sept. 26-28. Red Lion Hotel, San Jose, CA. Contact Jeff Silha, IDG World Expo, (800) 225-4698 or (508) 820-8628.

WESCON '94, Sept. 27-29. Anaheim Convention Center, Anaheim, CA. Contact Joan Carlisle, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (310) 215-3976; fax (310) 641-5117.

OCTOBER

1994 IEEE International Test Conference (ITC), Oct. 2-6. Sheraton Washington Hotel, Washington, DC. Contact Doris Thomas, International Test Conference, 205 Tennyson Ave., Suite C, Altoona, PA 16602; (814) 941-4666; fax (814) 941-4668.

Antenna Measurement Techniques Symposium '94, Oct. 3-7. Hyatt Regency, Long Beach, CA. Contact James P. McKay, The Aerospace Corp., M1/135, P. O. Box 92957, Los Angeles, CA 90009; (310) 336-1596; fax (310) 336-6225.

Far East Tour 1994, Electronics & Computer Shows, Oct. 4-17. Japan, Taiwan, Hong Kong, Korea, China, Singapore. Contact Ellen Wong, Commerce Tours International Inc., 870 Market St., Suite 920, San Francisco, CA 94102; (415) 433-3072; fax (415) 433-2820.

CD-ROM Expo/Boston, Oct. 5-7. World Trade Center, Boston, MA. Contact Mitch Hall & Associates at (617) 361-2001.

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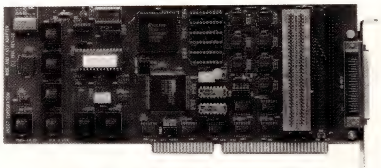

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INTELLIGENT NETWORKS

For this issue, Communications Editor Lee Goldberg took on a daunting task: He peels off layer upon layer of phone-company jargon in an effort to find out what The Intelligent Network is all about. Because I was primarily responsible for making this assignment (which some might describe as cruel and unusual punishment), I think it's worth noting up front that he did his usual fine job.

In my view, *Electronic Design* has many responsibilities to its readers. Our primary mission is to bring the latest technical information to our readers' attention and help them understand its significance. In an industry as dynamic as the electronics industry, we can easily spend all of our time doing just that. But I also believe it's incumbent upon us from time to time to shed light on subjects that may not be exactly what their proponents claim.

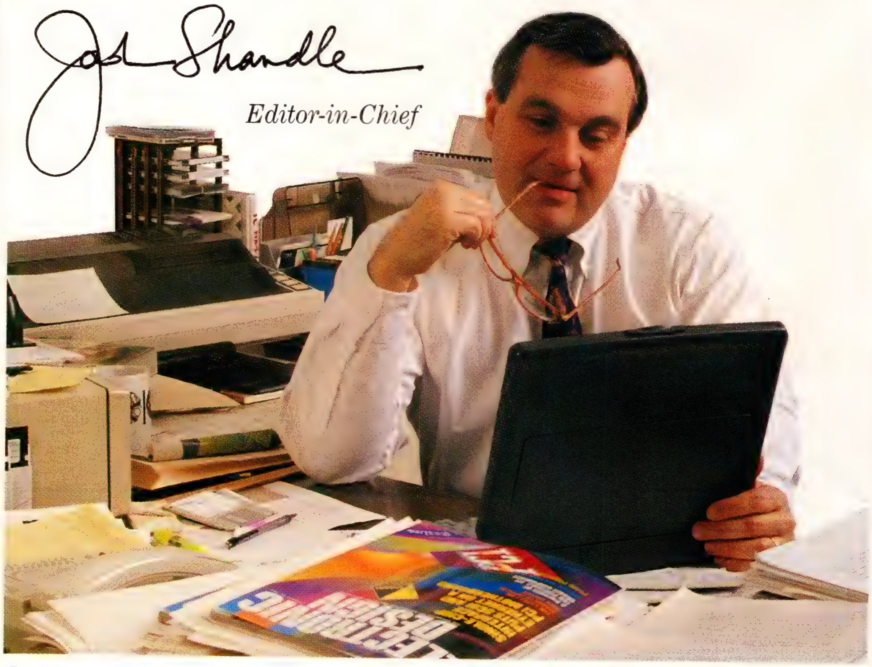
The phone company (although there is no single phone company anymore—just seven sisters that all think about the same) is a good place to look for these strange creatures that are one-third technology, one-third marketing, and one-third to-be-announced. Remember the Integrated Services Digital Network? It has supposedly been ready for prime time since the early 1980s, but only now is it being deployed. In retrospect, I think the media should have been more active in tracking down the problems that held ISDN back. For the most part, the problems were tied to the business end, such as the time it would take phone companies to set up tariffs and billing procedures. Someone who looked solely at the technology got roughly one-third of the picture.

I'm sure some companies that paid close attention to what they read in the media and to what some analysts and forecasters were saying about ISDN "way back when" placed a bet on ISDN and suffered financially as a result. Let's hope that doesn't happen with the Intelligent Network. In his article on the Intelligent Network, Lee solicited an adversarial view. Maybe having so much intelligence in the network is not the best way to serve the needs of consumers. It's certainly a point worth considering. One thing seems clear: Putting functionality and intelligence in equipment such as PBXs and computer cards (not the network) will probably better serve our readers' interests.

The phone companies want to play a bigger role in the information society other than just providing an "information pipe." The Intelligent Network is one part of their strategy to get there.

Jon Shandle

Editor-in-Chief



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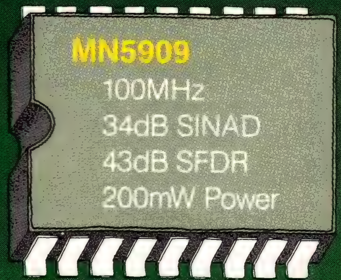

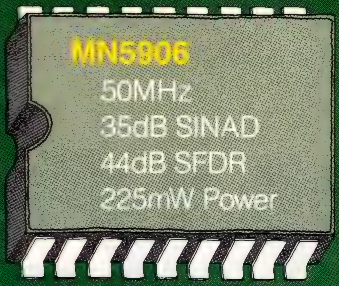

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KNOW YOUR HIGH-SPEED INTERCONNECTS

In the design of extremely high-speed networks such as Fibre Channel, where data rates can exceed 1 Gbit/s, it's become critical to characterize the data-transmission performance of I/O paths. Component suppliers have tried to help by focusing on issues such as crosstalk, impedance matches and changes to them, attenuation, and electrical length, but such parameters are only parts of the bigger picture. It's time to take a more holistic approach to characterization of the I/O path.

Telecommunication engineers working with long-haul cables have long been acquainted with a cable-characterization technique called eye-pattern analysis, in which a differential signal is driven through the cable and examined at the terminus with a sampling oscilloscope. As random data bits are superimposed on top of each other on the oscilloscope screen, an "eye" pattern takes shape. Eventually, the cable's limitations cause that "eye" shape to narrow until errors begin to creep in as intersymbol interference.

Engineers at W.L. Gore & Associates Inc., Newark, Del., are applying eye-pattern analysis to a new family of high-data-rate cables that's compatible with all 2-mm backplane connector systems. Doing so helps determine the impact of design options on the total transmission performance of the complete I/O path. According to Craig Theorin, a product specialist at W.L. Gore, eye-pattern degradation represents a severe bottleneck in high-speed systems requiring cable runs of any significant length. "At these data rates, moving past five feet or so of cable is what you might call a 'long' run," said Theorin. "If you're using a slow data rate, like Ethernet, cable length is less significant. But if you're using a backplane connector with a 2-mm pitch, you can only use so big of a cable. Then 'long' becomes a much smaller number."

DAVID MALINIAK
COMPONENTS & PACKAGING

Coupled with the trend toward higher data rates is another trend toward lower-voltage-swing logic transitions. According to Mike Scott, product manager for the 41-Series of line drivers, receivers, and transceivers from AT&T Microelectronics, Allentown, Pa., many designers are exploiting the lower voltage swing of the pseudo-ECL output level (about 1 V) used by drivers and receivers like the 41-Series instead of the TTL-type interface, which swings about 2 to 2.5 V. This shift in transition levels brings good news and bad news. On the plus side, a differential pair is now switching at lower voltages, which means lower amplitude signals and less radiated noise. Skew is also reduced for higher performance.

But the minus side is that at lower transition levels, the cable is even more of a factor in ensuring that signals traverse its length without error. So in this scenario, a scheme for more stringent characterization of the I/O path, such as the one adopted by W.L. Gore, becomes even more necessary. This is illustrated by the fact that at cable runs up to about 10 meters, the data rate the 41-Series drivers can sustain is limited by the device itself, says Scott. That rate ranges to 400 Mbits/s. But at longer lengths, cable impedances and capacitances begin to reduce the overall system data rate, making the rate line-dependent.

In general, it seems as though engineers are more aware than ever of the impact of the interconnections they design into their systems. According to Fabrizio Zanella of Teradyne Connection Systems, Nashua, N.H., more and more buyers of Teradyne's 2-mm backplane systems request complex Spice models of the interconnections. Such multiline or matrix models typically represent 36 pins and enable the user to choose which pins to define to ground and determine what the crosstalk would be between the signal lines. In addition, more interconnect manufacturers are making such detailed models available to customers. Hopefully, suppliers and users of interconnects will continue to work together to help make high-end systems fall into place more easily.

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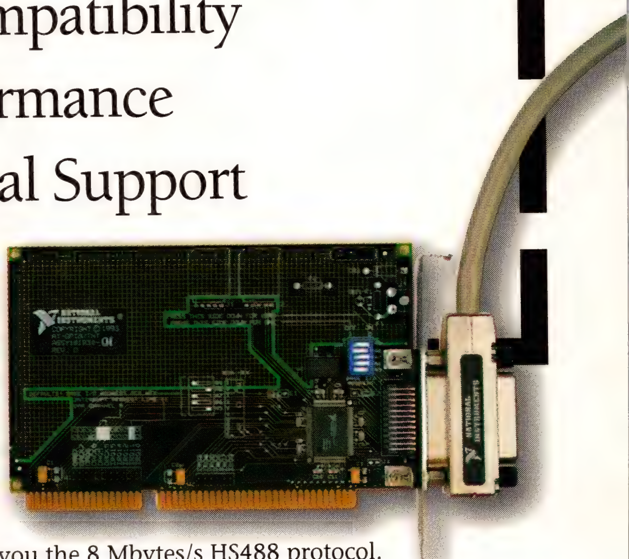
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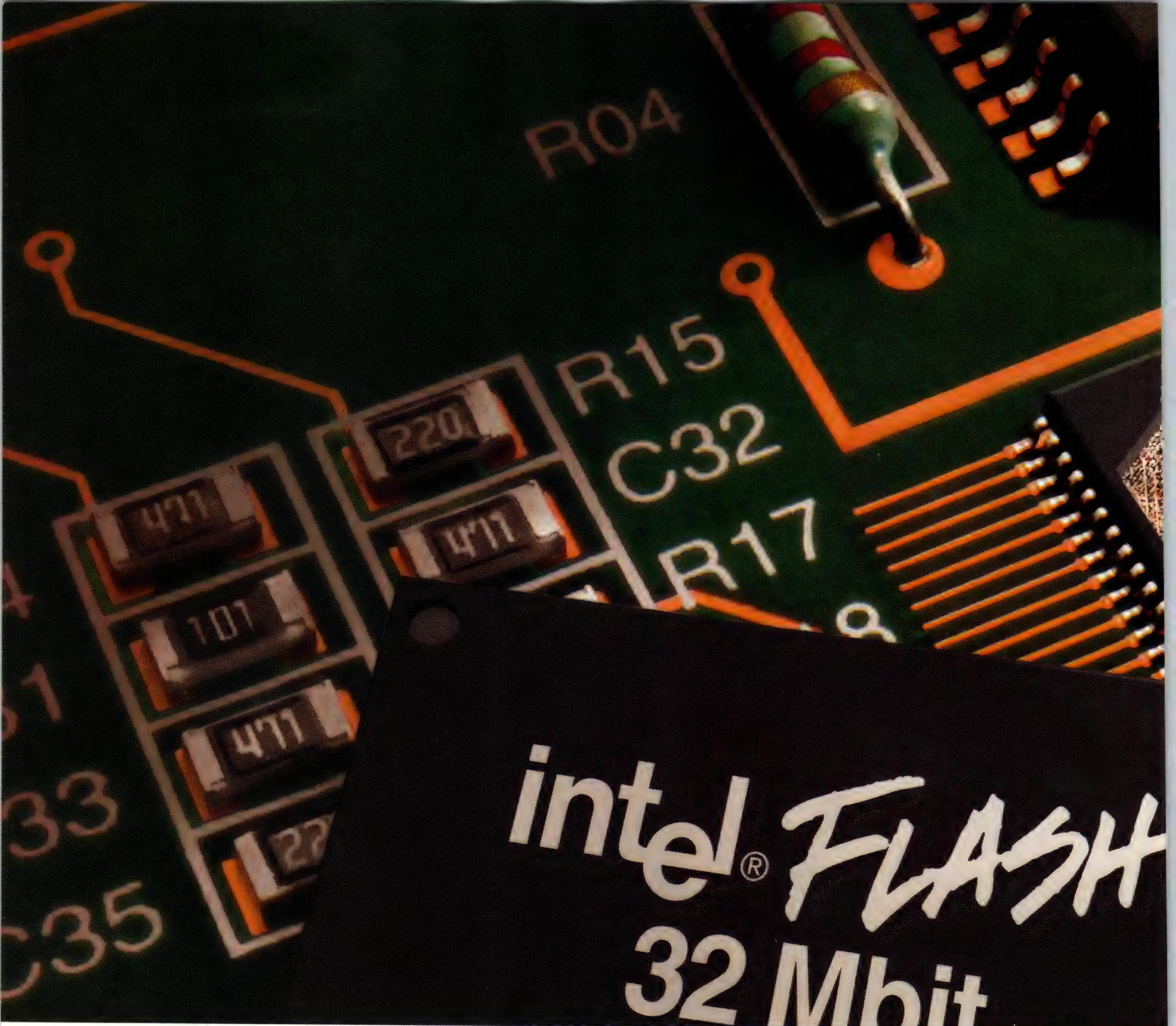

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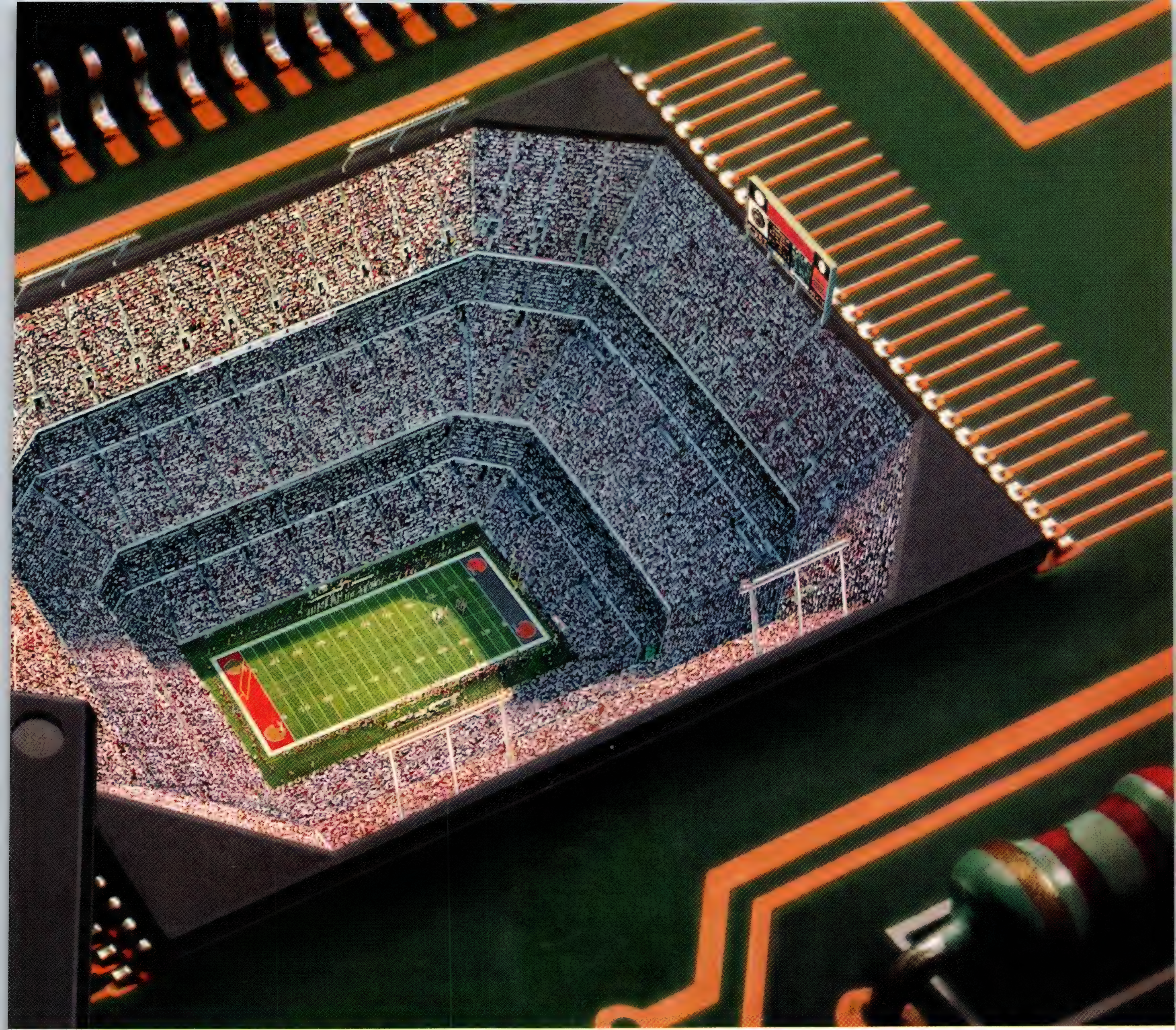

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UPCOMING MEETINGS

OCTOBER

1994 GaAs RED Workshop, Oct. 16. Wyndam Franklin Hotel, Philadelphia, PA. Contact William J. Roesch, TriQuint Semiconductor, (503) 644-3535 ext. 273.

1994 Wireless Circuits, Interconnection, and Assembly Workshop, Oct. 16-19. Paradise Valley, AZ. Contact Sharon Aspden, conference coordinator, Rogers Corp., 100 S. Roosevelt Ave., Chandler, AZ 85226; (602) 961-1382; fax (602) 961-4533.

5th International Conference on Signal Processing Applications & Technology, featuring DSP World Expo, Oct. 18-21. Infomart Conference and Exhibition Center, Dallas TX. Contact DSP Associates, 49 River St., Waltham, MA 02154; (617) 891-6000; fax (617) 899-4449.

Soft Ferrite Users Conference '94, Oct. 24-25. Westin O'Hare Hotel in Chicago (Rosemont) IL. Contact Magnetic Materials Producers Association, 11 S. LaSalle St. #400, Chicago, IL 60603; (312) 201-0101; fax (312) 201-0214.

Geoworks Technology Summit '94, Oct. 25-26. Hyatt Regency, Burlingame, CA. Call (800) 524-1857, ext. 1212.

1994 IEEE Nuclear Science Symposium (NSS), Oct. 30-Nov. 5. Norfolk, VA. Contact Lowell A. Klaisner, Stanford Linear Accelerator Center (SLAC), P. O. Box 4349, Mail Stop 30, Stanford, CA 94309; (415) 926-4463; fax (415) 926-3654.

LEOS '94, Oct. 31-Nov. 4. Sheraton Boston Hotel & Towers, Boston, MA. Contact Susan Evans, IEEE/LEOS, 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855; (908) 562-3896; fax (908) 562-1571.

NOVEMBER

16th International Conference of the IEEE Engineering in Medicine & Biology Society, Nov. 3-6. Omni International Harbor Hotel, Baltimore, MD. Contact Steve Marlin, Meeting Management Inc., 2703 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444.

1994 IEEE International Conference on Computer-Aided Design (ICCAD), Nov. 6-10. Red Lion Hotel, San Jose, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334.

1994 IEEE Global Telecommunications Conference (GLOBECOM '94), Nov. 27-Dec. 1. Fairmont Hotel, San Francisco, CA. Contact Terry Kero, Sprint, 1 Adrian Ct., Burlingame, CA 94010; (415) 375-4338; fax (415) 375-4079.

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TECHNOLOGY NEWSLETTER

GREEN MICRO LASER BOASTS SMALL SIZE

A recently introduced green-wavelength micro laser represents a major breakthrough in laser technology in terms of size, power, and cost. Developed at Uniphase Corp., San Jose, Calif., the micro laser combines infrared-diode laser energy and a proprietary crystal formulated using a new material known as vanadate. By reducing the long wavelength of the already developed red-diode laser, scientists are able to produce the shorter wavelengths required for a green laser. The micro laser is approximately 1 in.^{3} in size, and is 100-times smaller than other conventional devices. It has a power range of 5 to 10 mW at a cost of $5000 to $12,000, including power supply. These features make it ideal for applications in the biomedical and printing industries. It is anticipated that the micro laser will play a key role in the development of laser-based RGB systems for color printing and high-definition displays. Currently, work is being done by the company to develop a blue-wavelength laser. Call Uniphase at (408) 434-1800. *CA*

MULTILAYER POLYMER SUITS LARGE-AREA MIRRORS

Through mutual cooperation, Optical Data Associates (ODA), Tucson, Ariz., and the Materials Science & Development Laboratory of Dow Chemical Company, Midland, Mich., have characterized Dow's unique extruded microlayer polymer. Currently, the new polymer is being used in the design of large-area mirrors. One mirror design, for example, reflects visible light but is transparent to infrared radiation. It is expected that such a mirror could find its place in projection systems, medical lighting, fixtures, and energy-conservation glazing. The patented material is made by driving resins with diverse refractive indexes through a specialized extruder, forming a complex structure. Because this structure can consist of hundreds to even thousands of optical layers, and it is as rugged as the polymers from which it is made, no additional substrate is required for support. Due to the nature of its construction, the polymer also eliminates any problems with adhesion. In addition, the extrusion process used to formulate the multilayer polymer is inexpensive, compared with conventional layer-deposition processes. Consequently, it is ideal for a number of large-area applications. For further information, contact Dr. Michael R. Jacobson at (602) 748-7333. *CA*

CONSORTIUM MONITORS SEMICONDUCTOR INDUSTRY

The Ultra Clean Technology Research group of Tohoku University, Sendai, Japan, is the most recent addition to a joint U.S.-European research program, consisting of the BOC Group, Murray Hill, N.J.; MCNM Research Consortium, Research Triangle Park, N.C.; and the Interuniversity Microelectronics Center, Leuven, Belgium. The international consortium is dedicated to using in situ monitoring technology to look at semiconductor gas contamination effects on chip yield for cost-of-ownership analysis. Past research has focused on gas purification and analysis, and advanced semiconductor processing, resulting in valuable feedback on the performance of new grades of specialty gases and equipment and on-site nitrogen generators. Future work will examine ways to improve the accuracy of semiconductor chip yield production models. Specifically, the BOC Group is developing in-reactor methods of gas analysis at MCNC for improved characterization of semiconductor manufacturing. MCNC is refining the Sematech total cost-of-ownership models, which allow chip makers to rate the value of specific improvements in gas processing by examining chip yields and economic factors. Both IMEC and Tohoku University will coordinate to utilize the analytical techniques on several advanced processes in their respective fabs. For further information, contact Martha L. Eckert at (908) 771-1882. *CA*

SANDIA TO STUDY STORAGE SYSTEM

Sandia National Laboratory, Albuquerque, N.M., and IBM Federal Systems Company, Houston, Texas, have combined efforts to develop a high-performance storage system (HPSS). The results of their study, as part of a $3.7 million Cooperative Research And Development Agreement (CRADA), are expected to lead to the development of a storage system that will function effectively with a wide range of massively parallel processing systems. It is anticipated that this system will be used in high-performance computer network environments, particularly for the transfer of large files between supercomputers and storage at high speed. Future efforts will focus on testing a general-purpose high-performance, distributed, hierarchical storage system architecture, and developing a new storage system in the areas of network-attached storage devices, multi-

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ple dynamic distributed hierarchies, storage-system management and security, and layered access to storage-system services. For more information, contact Sandia at (505) 844-7767. *CA*

ALLIANCE PROMISES NEXT-GENERATION LCD

A recent alliance between Optrex America (Plymouth, Mich.), Optrex Corp. (Tokyo, Japan), and Motif (San Jose, Calif.) will focus on the development of next-generation passive-matrix LCDs. The LCDs will incorporate an innovative driving technology with display panels that provide both high contrast and fast response. In addition, the displays will feature a new passive-matrix technology, Super Twist, which provides image quality comparable to active matrix thin-film transistors (TFTs) but at a substantially lower cost.

Both Optrex and Motif developed different technologies—Multi Line Selection (MLS) and Active Addressing (AA), respectively—to offer improved response times and contrast ratios targeted to reach a performance level comparable to TFT. But by combining their approaches (under the trade name MLS-AA), the best of both methods is accomplished. The new MLS-AAs will differ from conventional-driving LCDs in that they can simultaneously select and scan multiple lines. The complicated pulse waves caused by the multiple scanning will be controlled by ICs with calculation functions, contributing to only a small cost increase over conventional LCDs. With a response time fast enough to handle video rates, it's expected that the MLS-AAs will be used in notebook and subnotebook computers, as well as PDA applications. For more information, call Optrex America at (313) 416-8500. *CA*

BRAIN MODEL ASSISTS VIDEO COMPRESSION

Through research conducted by the scientists at Stanford University, Stanford, Calif., the normalization model on how the brain processes visual images has been successfully tested with monkeys. A modified version of the linear model proposed in 1962, the model accurately predicts how the brain cells in the primary visual cortex respond to various light patterns. It effectively explains the response properties of neurons in the primary visual cortex, as well as the appearance of certain optical illusions. The normalization model suggests that while individual neurons add and subtract the neural signals they receive, the neuron's activity level is partially suppressed by the cumulative activity of a large number of other cortical neurons. In effect, each neuron's response is divided by a quantity proportional to the activity of surrounding neurons. Thus, each neuron is normalized with respect to the variation in the light intensities in the retinal image.

The model, proposed by assistant professor David J. Heeger of Stanford's Psychology Dept., may help engineers working to develop a means of compressing video images for transfer over computer and cable TV networks. One factor in accomplishing this task is the ability to identify information in the images that can be deleted. It is believed that the normalization model will be used to predict which information can be removed with the least amount of degradation. For additional information, contact David F. Salisbury of the Stanford University News Service at (415) 725-1944. *CA*

AUTOS MAY GET VOICE NAVIGATION

A voice-activated audio navigation system may find its way into cars soon. AudioNav, currently under development by Amerigon, Monrovia, Calif., consists of a small electronic module and microphone connected to a compatible audio CD player. The CD contains all of the operating software, map data, and speech-recognition software needed to run the system. To hold this information, though, conventional CD players must first be modified to incorporate a manufacturer-installed connector. CD manufacturers who could contribute to this project are being investigated. The speech recognition technology, on the other hand, will be contributed by Lernout & Hauspie Speech Products, Woburn, Mass. The technology consists of integrated alphabet and isolated word speech-recognition technologies. It will eliminate the need for expensive, awkward, and potentially dangerous keyboards and display monitors. In addition, the technology can be run on a range of low-cost, general-purpose DSPs, and can operate effectively in auto environments at speeds up to 60 m.p.h. with open windows. The integrated AudioNav system will operate in a straightforward manner. Drivers simply spell out their current location followed by the intended destination. The system then loads the appropriate maps from the CD and calculates the optimum route. The driver can then prompt the system for directions by using a set of simple voice commands, such as "next," which prompts the system to offer respective parts of the route. While development of this product continues, it is anticipated that a commercial product will be available through consumer-electronic retail stores for between $500 and $600, not including the price of a CD player. Each CD map of a particular metropolitan area will retail for about $50. For more information, call Amerigon at (818) 932-1200. *CA*

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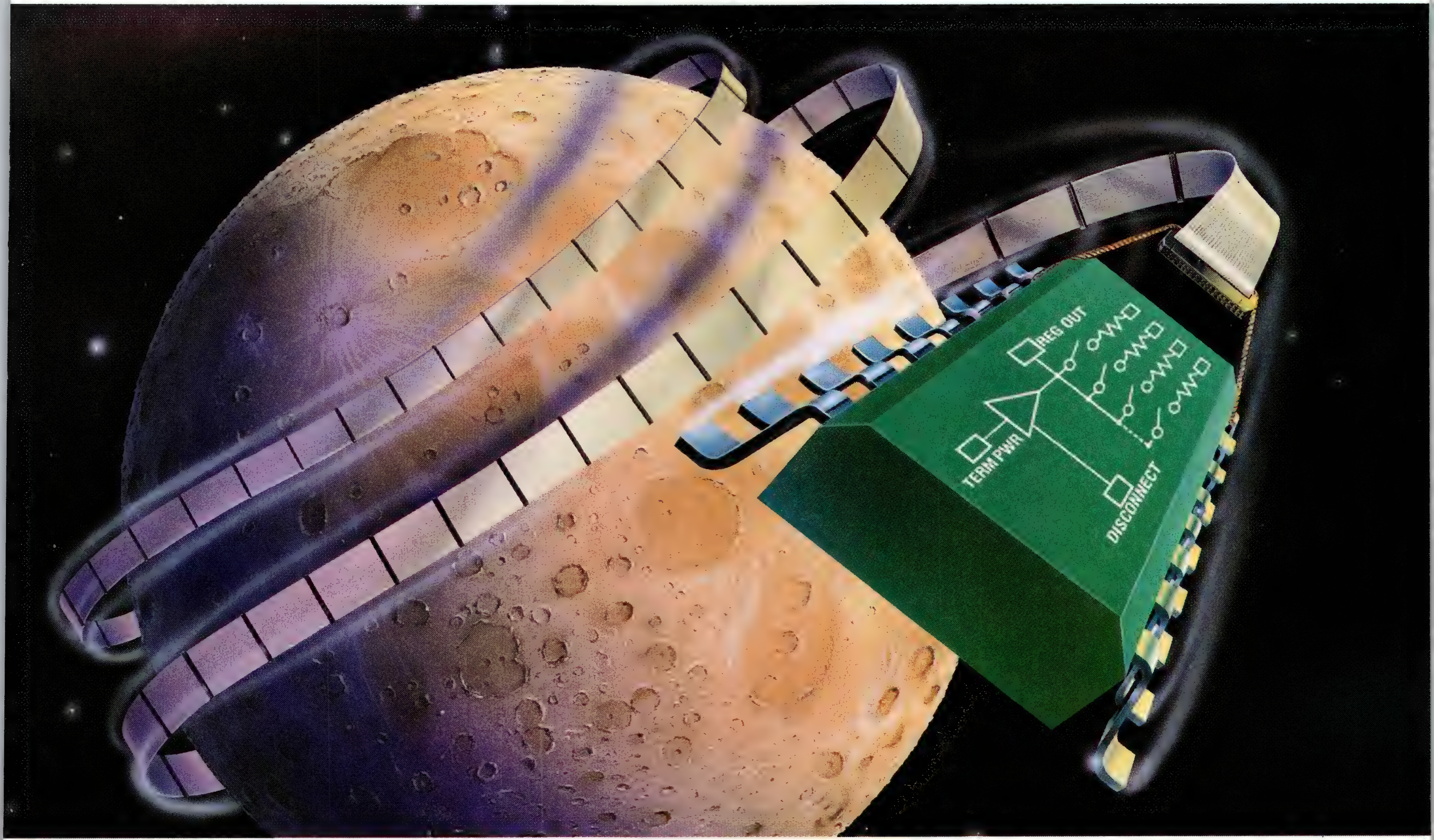

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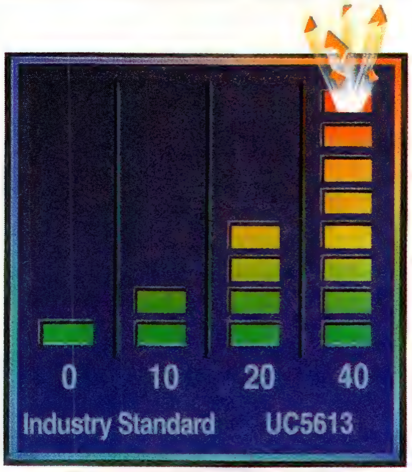

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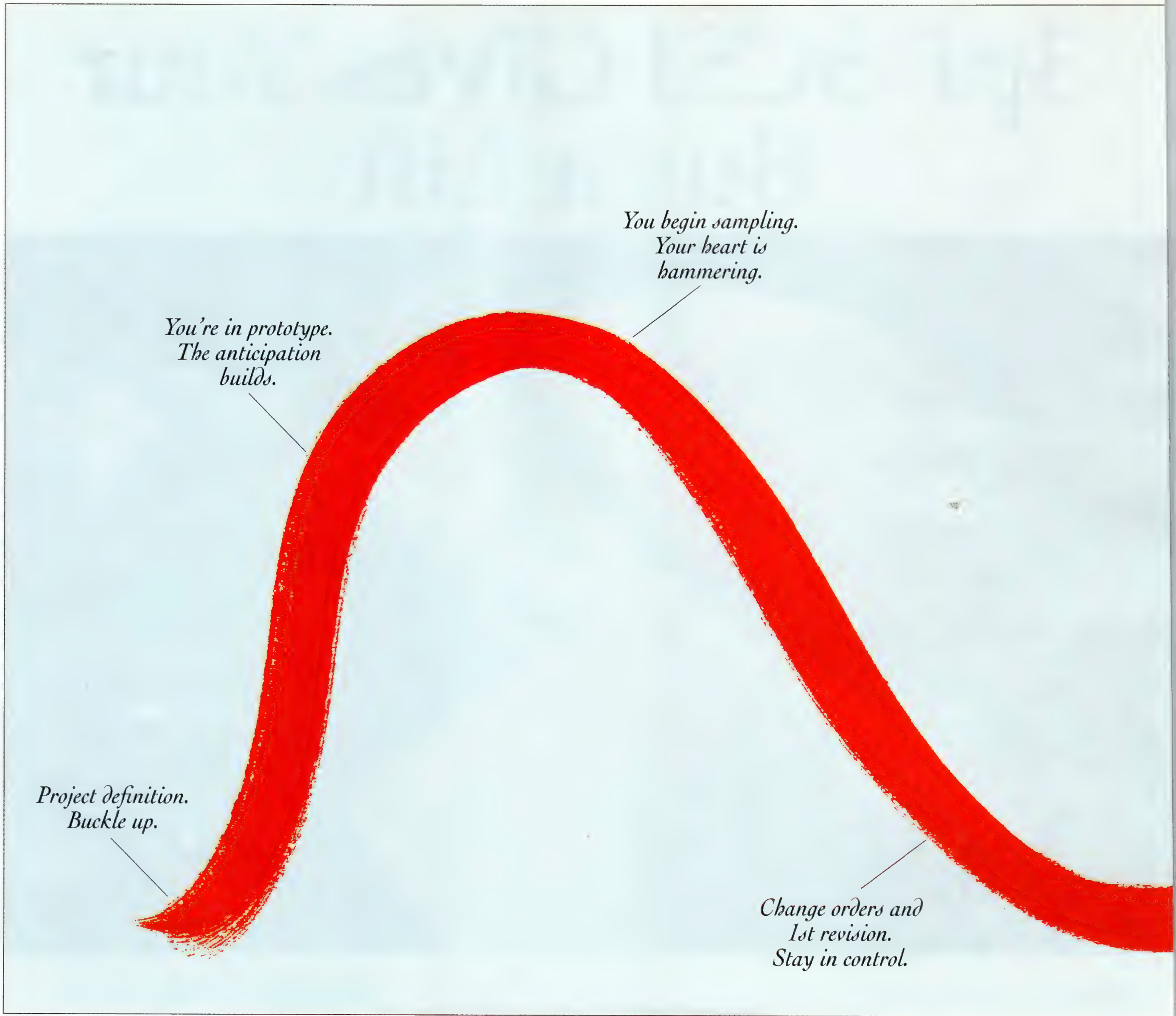
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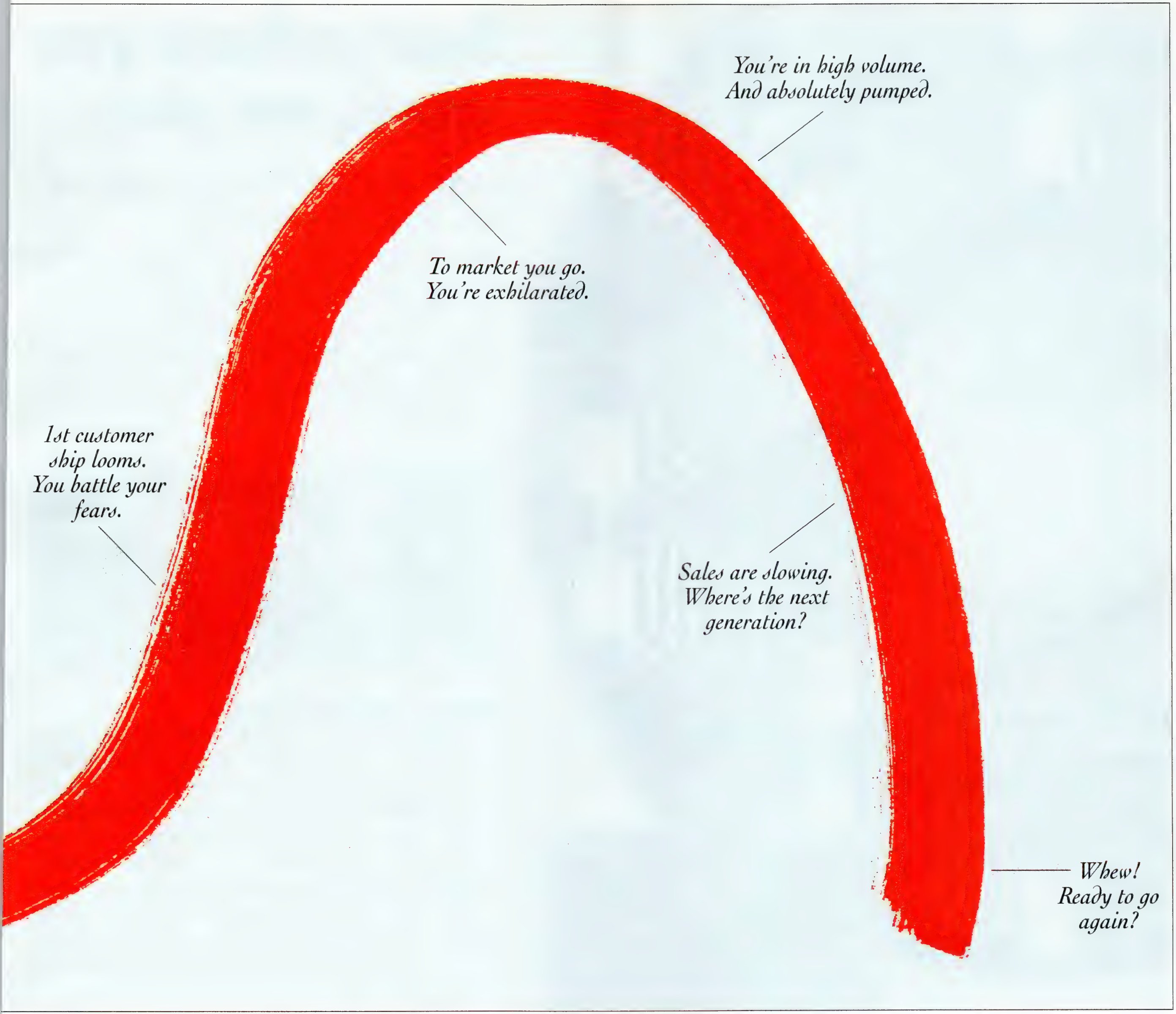
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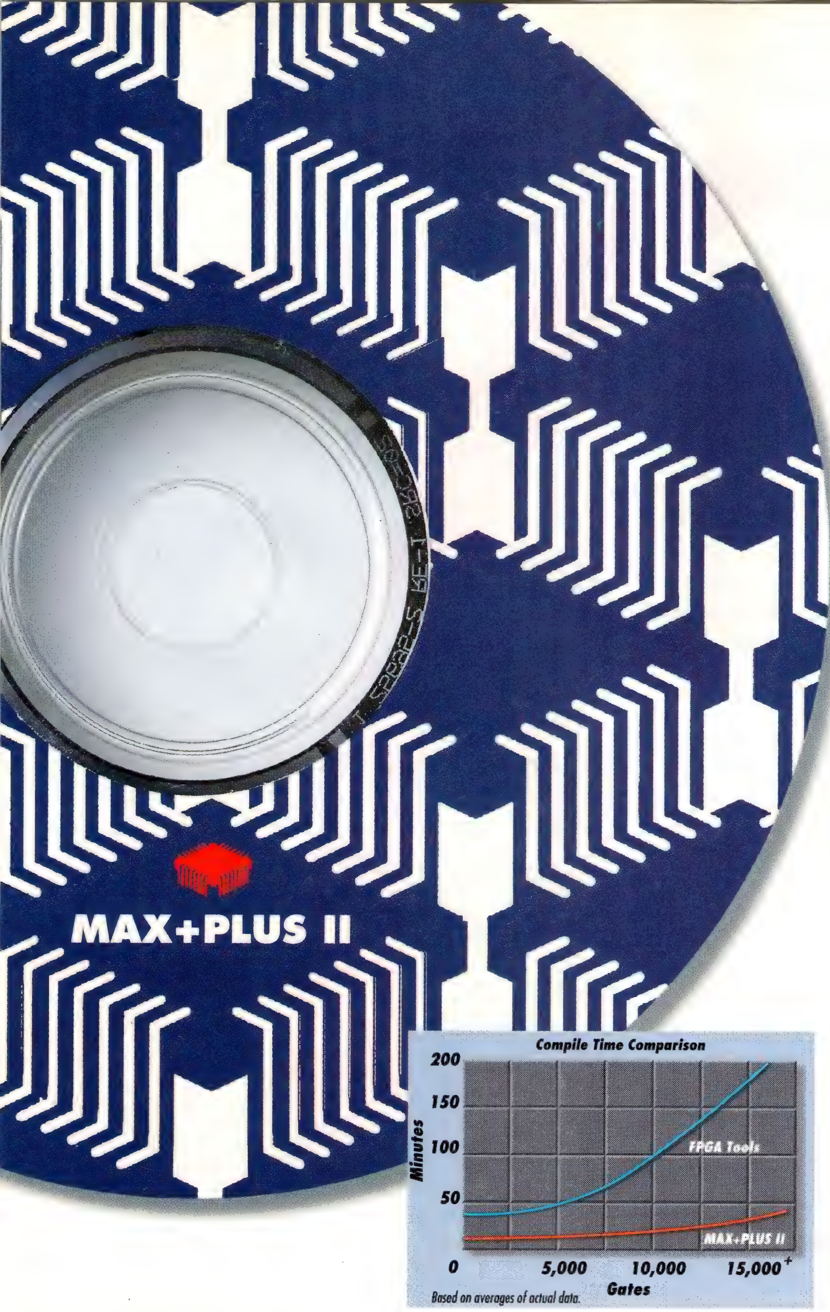

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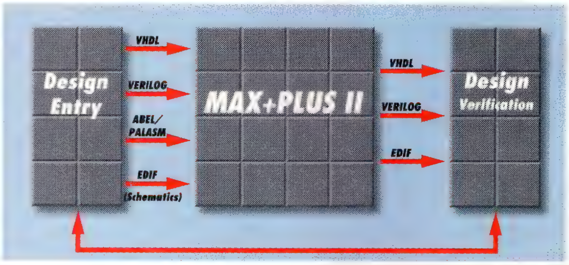

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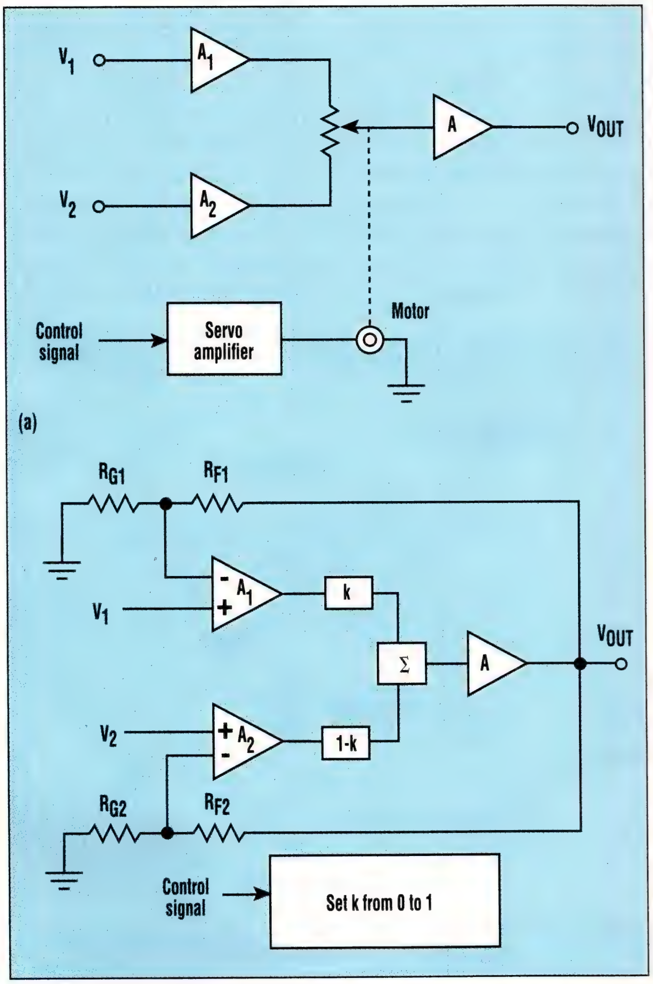
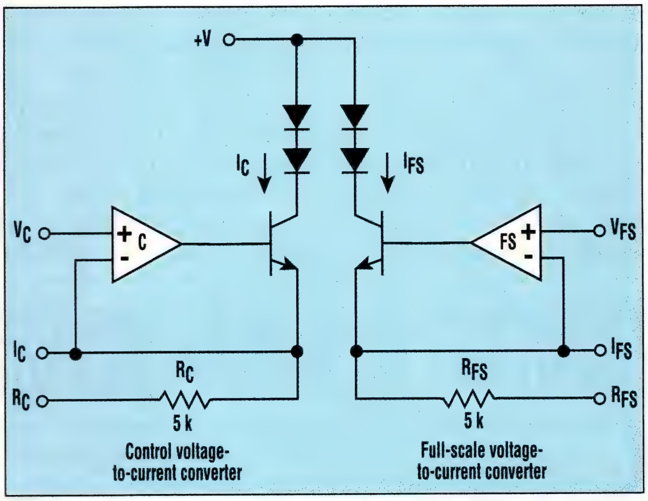
TWO CURRENT-FEEDBACK OP AMPS AND A LINEAR CONTROL CIRCUIT BUILD MONOLITHIC VIDEO FADERS

Faders in video systems are complex circuits, requiring linear control, a wide bandwidth, low distortion, and a dc output level independent of the control signal. In addition, accurate gain—unchangeable over temperature—is mandatory. Such parameters can be met with electromechanical approaches such as servo-driven potentiometers, which have their own drawbacks that can be overcome with a monolithic design. But cramming all this performance into on semiconductor IC (which must sell for about \$6.00 each in 1000-piece lots) is quite another matter.

This is what Bill Gross, op amp design manager at Linear Technology Corp. (LTC), Milpitas, Calif., was up against when he determined that the market needed a single-chip device and started developing the company's LT1251/LT1256 faders.

In a video system, a fader circuit dissolves one video signal (picture) into a second video signal (a second picture). An ideal fader looks like a "potentiometer" connected between the outputs of a pair of amplifiers, each buffering a separate video input signal *(Fig. 1)*. The output of the fader is taken from the "wiper" of the "potentiometer" *(Fig. 1a)*. The control signal moves the "wiper" from one signal source (V_1) to the other (V_2) in a linear manner. That is, when the control signal changes from zero to full scale, the wiper moves from one end of the potentiometer to the other, and the output signal changes from just V_1 to just V_2. When the control signal is at 50% of its value, the wiper is at the center of the "potentiometer", and the output (V_{OUT}) equals $V_1/2 + V_2/2$.

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A fader can be constructed, as shown in the figure, using an electromechanical servo-driven potentiometer. Though this approach represents a straight-forward design, albeit it complicated, it is expensive and the control channel is slow .

In the LTC video fader, the servomechanism is implemented with mathematically equivalent blocks k, 1–k, and the summation circuit Σ, where k is a constant which can have any value between 0 and 1 *(Fig. 1b)*. A pair of current-feedback op amps providing gains A_1 and A_2 handle the two inputs. For flexibility, the user sets A_1 and A_2 gains with external resistors. Since the op amps are current-feedback types, the resistors also set the bandwidth. For the ideal condition where external feedback resistor R_{F1} equals external feedback resistor R_{F2}:

$$V_{OUT} = (k)(V_1)(A_1)+(1-k)(V_2)(A_2)$$

where

$$A_1 = 1 + R_{F1}/R_{G1}$$

and

$$A_2 = 1 + R_{F2}/R_{G2}$$

The control circuit consists of two identical voltage-to-current converters, each of which contains an op amp (C and FS), an npn transistor, as well as a resistor (R_C and R_{FS}) *(Fig. 2)*. The voltage-to-current converter on the right generates full-scale current I_{FS}, and the one on the left generates the control current I_C. The constant k is the ratio of I_C to I_{FS} and ranges from a minimum of zero when I_C equals zero, to a maximum of 1 when I_C equals or is greater than I_{FS}.

The op amp in each voltage-to-current converter drives the npn transistor connected to its output until the voltage at the op amp's inverting input equals the voltage at its non-inverting input. If the open end of either R_C or R_{FS} is grounded, the voltage across it is the same as the voltage at the non-inverting input. The npn-transistor's emitter current is therefore equal to the input voltage divided by the value of the resistor. The collector current is essentially the same as the emitter current and the ratio of the two collector currents sets the gain.

Grounding R_C and R_{FS} and applying a 2.5-V full-scale reference to the V_{FS} input sets I_{FS} at approximately 500 µA *(see figure 1, again.)*. When the control voltage applied to the V_C input is negative or zero, I_C and k are zero. When V_C is 2.5 V or greater, I_C equals I_{FS} and k equals 1. The gain of the V_1 channel ranges from 0 to 100% as V_C increases from zero to 2.5 V, while the gain of channel two (V_2) moves in the opposite direction, from 100 to 0%.

The resulting faders with both channels configured for a gain of one sport small- and large-signal bandwidths of 30 MHz and a slew rate of 300 V/µs. Differential gain and phase run 0.1% and 0.1°, respectively, and total harmonic distortion runs 0.001% (at 1 kHz and k = 1). The bandwidth of the control-signal path is 10 MHz.

For additional information on the IC video faders, call Bob Scott at (408) 432-1900.

FRANK GOODENOUGH

Vibration Isolation Uses Piezo-Ceramic Elements To Yield Ultra-Quiet Plaforms

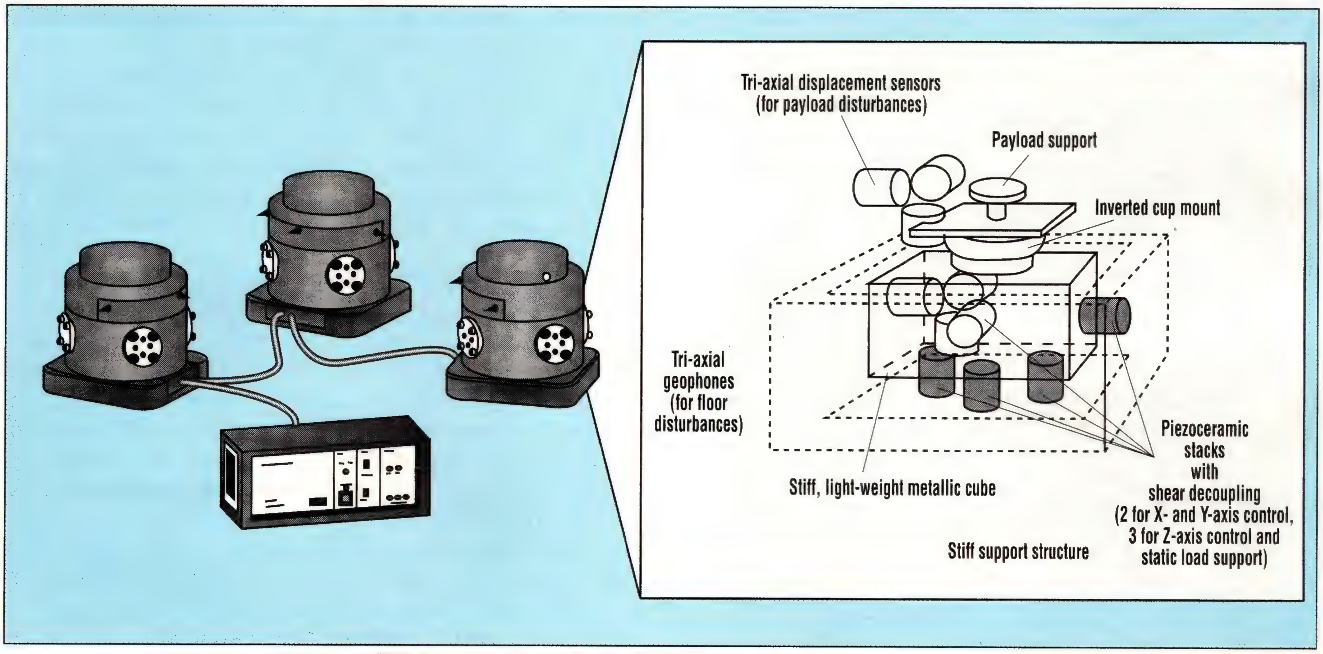
Companies that manufacture ICs using deep-submicron lithography have long battled to overcome limitations in lithography, diffusion, etching, and other process steps. But through it all, to get the most accurate results, the manufacturing and some of the test-and-measurement equipment itself must be shielded from minuscule low-frequency vibration sources (microinch displacements)—especially in the lithography subsystems. Now, an active compensation technique promises to cut external low-frequency vibrations by sensing them and then generating opposing motions that effectively negate the vibrations.

To perform the active cancellation, engineers at Barry Controls, Brighton, Mass., have designed a scheme employing piezoceramic motion elements and both geophone and other displacement sensors embedded in active pedestals. Either three or four pedestals (referred to as feet) are tied together over a bus that connects them to a user-interface controller.

Active vibration isolation starts at frequencies of about 0.3 Hz and can reduce the effects of vibration by a factor of five times over any other currently available active scheme. Furthermore, the scheme significantly improves the ability to reject payload disturbances. The system actually employs both active- and stiff-passive-isolation subsystems. The active system enhances isolation from 0.3 Hz to 200 Hz, achieving up to 99% isolation starting at 30 Hz. In combination, the two subsystems attenuate up to 99% of the total vibration throughout the total range of frequencies.

The multi-foot subsystem can be used to stabilize each piece of equipment, and can contain the stabilization cost to about $30,000 per piece of equipment. Larger systems that employ more active feet can be created—the only limitation for now is the power supply used in the user-interface controller that ties the feet together.

By keeping the stabilization cost low, manufacturers can eliminate one of the major cost factors when they build their big facilities, says Rick Earle, the active product business manager. For example, Earle continues, many of the advanced fabrication facilities


Tri-axial displacement sensors
(for payload disturbances)
Payload support
Inverted cup mount
Tri-axial geophones (for floor disturbances)
Piezoceramic stacks with shear decoupling (2 for X- and Y-axis control, 3 for Z-axis control and static load support)
Stiff, light-weight metallic cube
Stiff support structure

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isolate their equipment by placing the critical items on suspended floors. Those floors are, in turn, isolated from the frame of the building and mounted on shock-absorbing pillars. Such schemes are very expensive, costing millions of dollars to implement, and often require exhaustive geological analysis in a search for a factory site away from most vibration sources.

As device features go below 0.5 µm, most conventional vibration-isolation schemes just aren't effective enough, and besides, the cost of building large, very remote facilities increases to astronomic levels. Active compensation, then becomes an attractive alternative since it can be done very selectively and could greatly reduce the cost of new facilities or allow them to be closer to metropolitan centers, which are major sources of undesired vibration.

Each foot (pedestal) developed by Barry Controls employs five piezoceramic elements that perform the active vibration isolation—one for the X, one for the Y, and three for the Z direction. These piezo elements, explains Steve Shedd, the project engineering manager, are controlled with high-voltage commands as large as 800 V, which are generated by the integrated electronics. Sensor and compensation electronics complete the control system, all of which is housed in the foot. High-voltage commands, of course, cause the piezo material to slightly expand, thus creating an equal "move out of the way" motion to the sensed vibration.

The feet, are in turn, interconnected over a bus that collects data from each foot and provides the master computer used by the manufacturing facility with vibration data and real-time health monitoring *(see the figure)*. But, to ensure safe system operation, the intelligence, signal sensing and amplification, and high-voltage generation are all performed in each foot.

The design of the active compensation system starts with three velocity-sensitive geophones that are used to sense floor disturbances, explains Andrew Beard the senior development engineer. The geophones are mounted inside a metallic cube, which is, in turn, suspended on five piezoceramic stacks. Encasing the assembly on all sides but the top is a stiff support structure, through which the floor motions will be transmitted to the sensors.

In addition to the trio of geophone sensors, continues Beard, a second set of tri-axial sensors is used to detect payload motion relative to the cube. The payload support is attached to the suspended metal block through an elastomer mount. The second set of sensors detect elastomer deflection and their outputs are used to inertially damp payload motion.

In the geophones, a coil moves in relation to a fixed permanent magnet, generating small electric signals, which are amplified, analyzed, and used to control the piezo elements. The geophone signals are typically in the microvolt range. As a result, attention to circuit and physical layout details was necessary during the design stage, to ensure other system noise from signal sources didn't swamp out the small sensor signals.

Although one might assume that with such small signals, digital-signal processing might be the best approach, Shedd and his team members found that analog processing still offered good robustness and were less expensive to implement—at least for this generation. The design team, however, did employ DSP-based development systems to create the closed-loop control scheme.

The anti-vibration scheme can even eliminate vibration coming from within a piece of equipment such as a wafer stepper, mask-inspection system, or laser trimmer, which typically have X-Y stages that must move at high speeds and yet generate little or no vibrations. By placing the pedestals underneath the system, the active compensation will sense the stage movement and rapidly damp payload motions, thus preventing rocking. Such compensation allows the equipment to usually exceed the equipment manufacturer's own operating specifications, thus improving manufacturing productivity for fine-featured chips.

For more information, contact Rick Earles at (617) 787-1555.

DAVE BURSKY

PROPOSED FPGA BENCHMARKS REFLECT REAL-WORLD DESIGNS

An FPGA synthesis benchmarking proposal was recently submitted as a working document to the Programmable Electronic Performance Corp. (PREP) standards organization by Actel Corp., Sunnyvale, Calif. The proposal offers an alternative to standardized synthesis-benchmarking methodologies currently being considered by PREP Working Group-4 (WG-4). It received immediate endorsement from Exemplar Logic and Innovative Synthesis Technologies, two high-level design- and synthesis-tool developers.

Actel's proposal calls for the institution of methodologies that more accurately reflect real-world design challenges. It also responds to the concerns of synthesis-tool vendors that current benchmarks appear to inhibit them from demonstrating their best capabilities. PREP WG-4 has been chartered with defining a benchmark methodology for high-level design- and synthesis-tools in concert with implementation tools and target components from programmable-logic vendors.

Tom Todd, Actel's director of product marketing, explains that "high-level design and synthesis results depend as much on the manner in which the tools are operated as they do on the core algorithms of the tools themselves. It's more like playing a musical instrument than playing music on a CD player" he explains.

The Actel proposal urges that component vendors, synthesis vendors, and customers be invited to submit real-world designs as benchmarks. More specifically, Actel's proposal recommends that:

- Benchmark circuits must be of sufficient density to demonstrate the capabilities of high-level tools.
- Implementation methodology must allow use of any and all synthesis tools and methodologies available to engineers.
- Each circuit must use any five of nine existing PREP benchmark circuits

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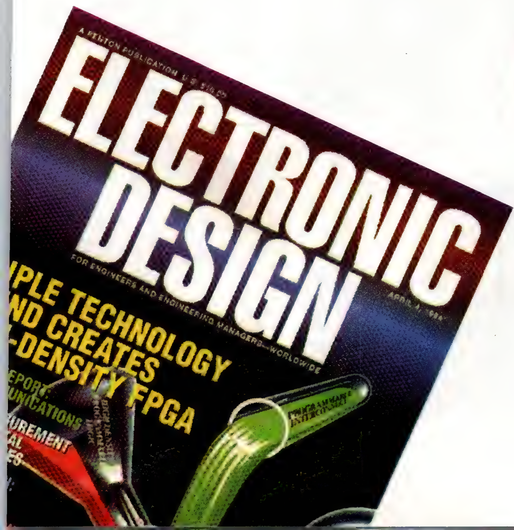

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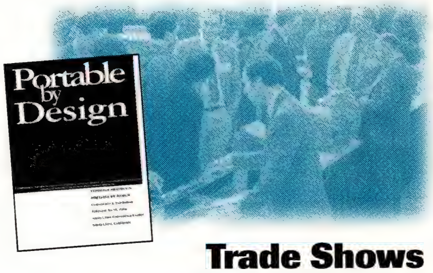

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as building blocks within the context of real-world design.

- Data reporting must require measurement of the performance of the real-world design in the context of its target system.
- The tools used must be generally available to engineers, and the methodologies used must be outlined in user documentation.

Dennis Nye, Actel's vice president of marketing, points out that it's important to improve algorithms, technology libraries, methodologies, and links between synthesis tools and tools developed by vendors. The Actel benchmark proposal, he asserts, allows for demonstration of those improvements as they evolve over time.

LISA MALINIAK

ADVANCED BALL-GRID ARRAY ADDRESSES COST AND SIZE ISSUES

The ball-grid-array (BGA) package is quickly gaining in stature among manufacturers and users of fast, high-power and high-I/O devices such as microprocessors, PLDs, and ASICs. But for many systems houses, the ceramic BGA is too large, heavy, and expensive. Amkor Electronics Inc., Chandler, Ariz., has developed an ultra-thin, lightweight BGA that takes some novel twists to address these and other issues of concern to high-volume assemblers.

The SuperBGA package's assets are many and are led by a thermal resistance of less than 10°C/W (θ j-a) and 0.3°C/W (θ j-c) for a package that measures 35 by 35 mm and has 352 I/Os, according to modeling data. The package permits signal speeds of up to a frequency of 1.5 GHz. In terms of size and weight, the typical SuperBGA package measuring 27 by 27 mm with 256 I/Os has a mounted height of 1 mm and weighs 2 grams.

Some BGAs mount the die on a pc-board-like substrate and run the traces through the substrate to the solder balls on the other side. In the SuperBGA package, the die is mounted in a cavity in the substrate on the same side as the balls are, which are thermosonically ball-bonded with gold wire to the die from a bond tier on the substrate's periphery (*see the figure*).

This, according to Amkor, shortens the paths from the die to the solder balls and reduces capacitance and inductance. The chip and cavity are then filled with a liquid resin. Typical line and space widths are 0.075 to 0.100 mm.

In other design options, vias are used to make electrical or thermal connection of multilayer designs with up to five metal layers. Construction is with a bismaleimide triazine dielectric separating signal layers. The dielectric offers a constant of 4.1 to 4.3

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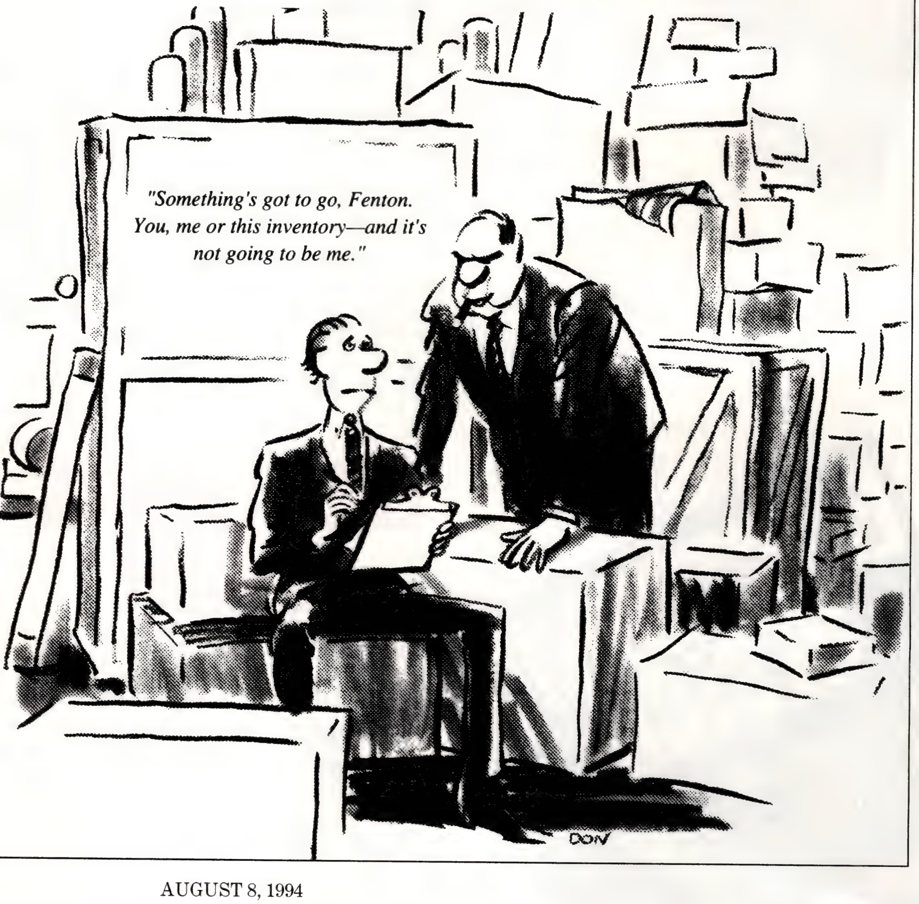
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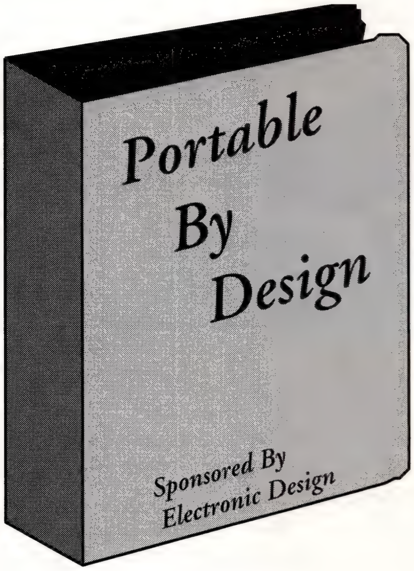

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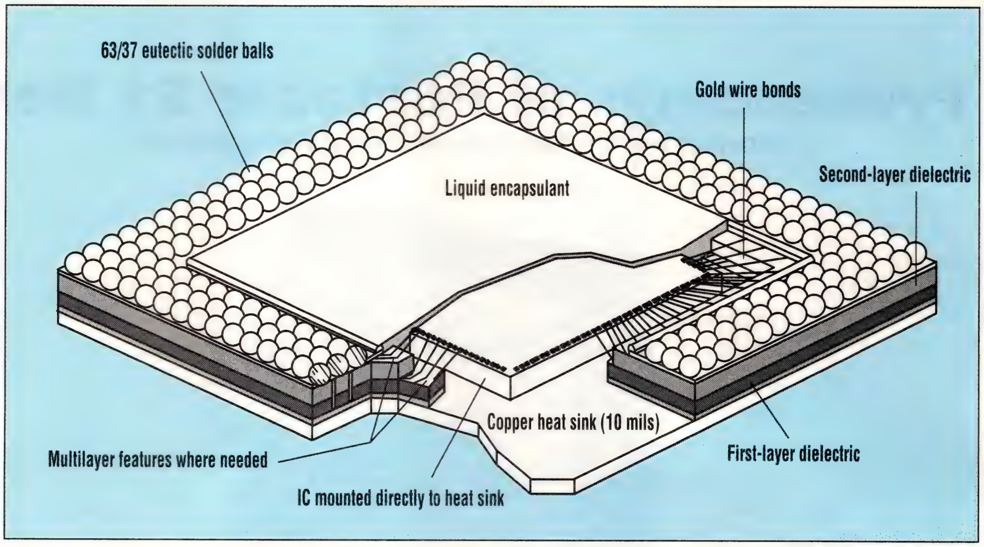
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Copper heat sink (10 mils)
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First-layer dielectric
IC mounted directly to heat sink

at 1 GHz.

Another advantage of placing the balls on the same side of the substrate as the die is in routing. Systems houses can easily route from the board to the SuperBGA package using 4-mil traces rather than having to use 1 mil or less in some cases.

A key feature of the package is direct attachment of the chip to a thin, yet highly conductive copper heat sink. This heat sink covers the entire top surface of the package to provide an optimal path for heat dissipation as well as an effective EMI/RFI shield. The high θ j-a specification is the result. Silicon die, in some cases, have 120°C junction temperatures and 40°C ambient operating temperatures. Using a 10°C/W θ j-a figure yields a calculated power-handling specification of about 8 W. Dissipation can be as high as 12 W depending on conditions. Amkor is working with Aavid Engineering Inc., Laconia, N.H., to develop heat sinks that will be compatible with the SuperBGA package and will improve its thermal-dissipation factor.

A complete family of ball counts from 20 through 680 and body sizes from 7 by 7 through 51 by 51 mm will comprise the SuperBGA family.

For more information on the advanced ball-grid array, contact Amkor at (602) 821-5000.

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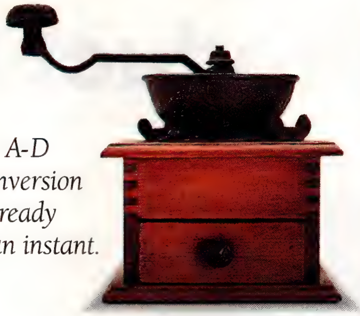

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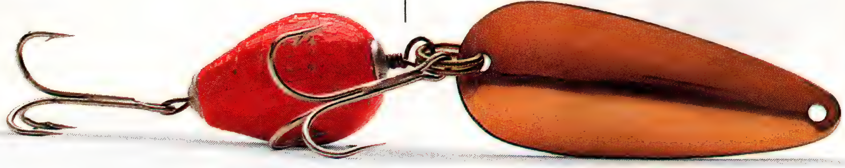

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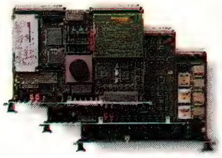

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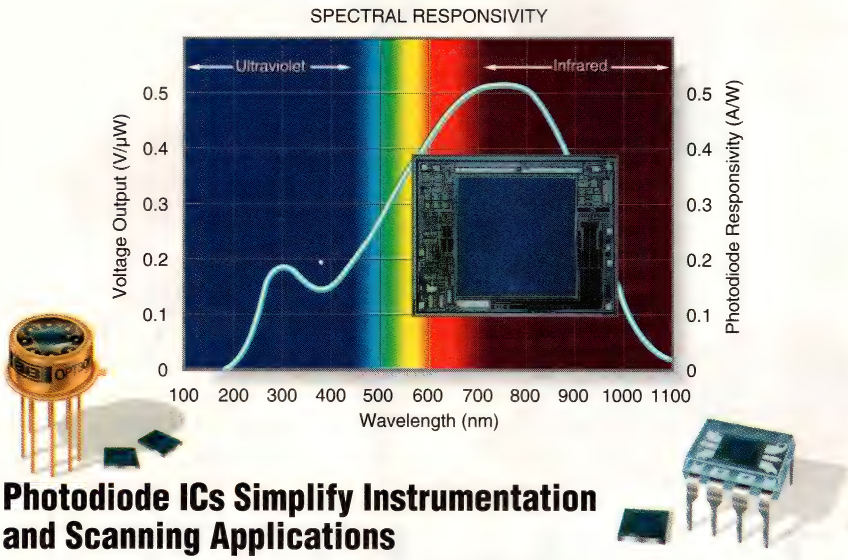

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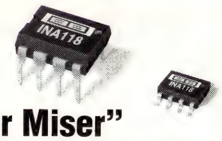

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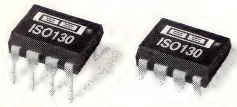

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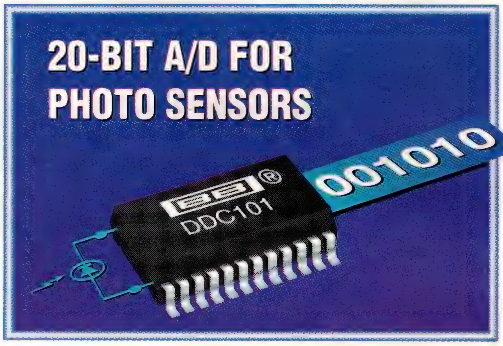
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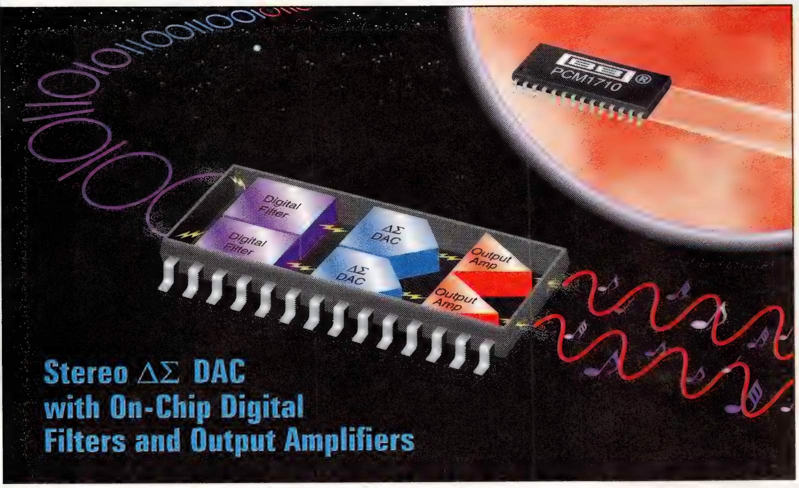

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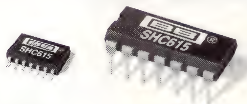

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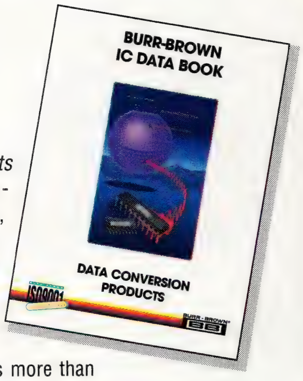

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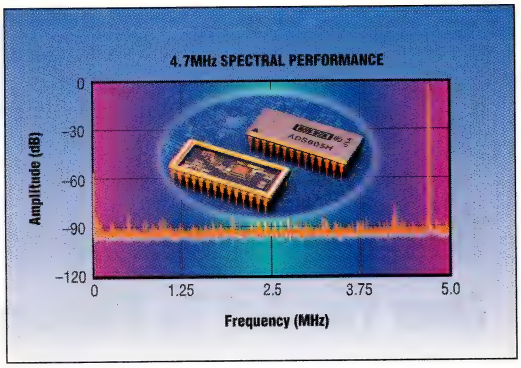

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DUAL 180-V/600-V GAAS POWER RECTIFIERS UP THE EFFICIENCY OF HIGH-FREQUENCY SWITCHERS; 180-V UNITS HANDLE 20 A, 600-V UNITS 3 A.

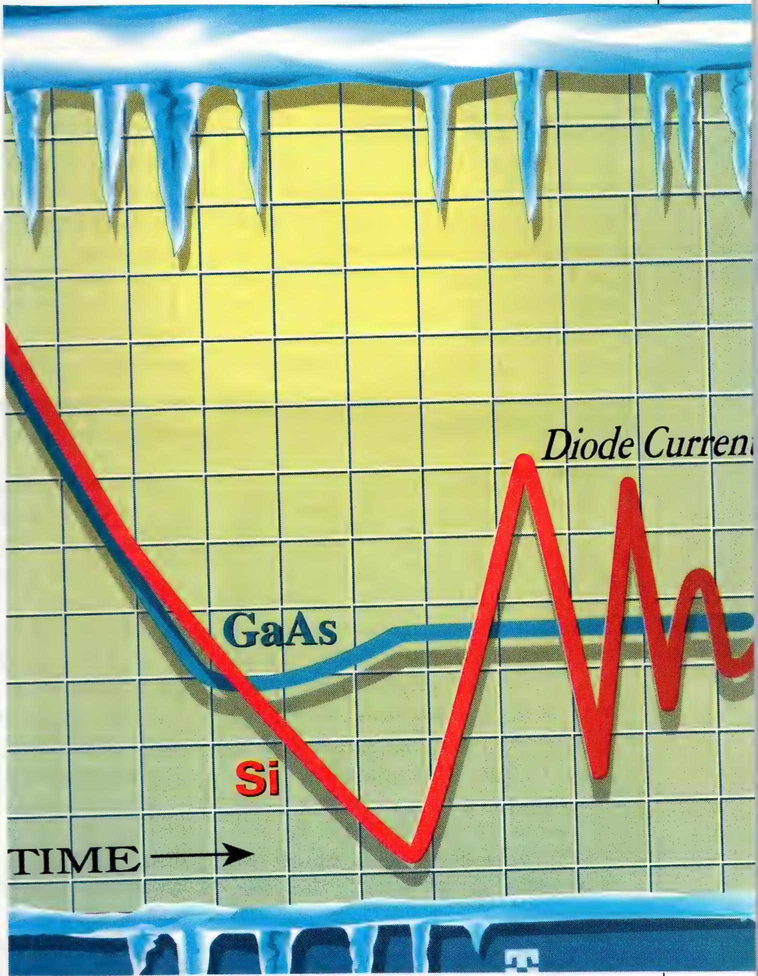
DUAL 180-V GAAS SCHOTTKY DIODE RECTIFIES 10 A/LEG

FRANK GOODENOUGH

Innovation in the power-control/management/quality arena is driven by power density—the number of watts per cubic inch. The power-density push exists whether the application is a notebook PC, a modular distributed power supply for telecommunications, or solid-state drivers for a fractional-horsepower three-phase induction motor. In all of these applications, switching frequencies climb above a few hundred kilohertz to reduce the size of the passive parts. But at these frequencies, silicon rectifiers in the circuit severely limit efficiency, particularly if the rectifiers must handle reverse voltages of 200 V or more. And, efficiency equates to power density. The heat generated by conduction, switching, and other losses limits just how tightly components can be squeezed into the package, and how much structure must be used to remove that heat from the ultimate heat sink.

With that in mind, researchers at Motorola several years ago started to develop a gallium-arsenide (GaAs) power Schottky-diode rectifier technology *(see "Motorola's GaAs skunk works," p.* **XX***)*. The results of that work are finally coming to fruition. The first device to emerge, a 180-V dual GaAs Schottky diode, handles 20 A continuously (each diode handles 10 A). Dubbed the XGR2018CT, it will be followed by 600-V rectifiers.

During the R&D phase, the Motorola team demonstrated GaAs diodes with breakdown voltages of over 1000 V and fabricated experimental rectifiers that can handle from 100 to 800 V—all with soft, reverse-recovery times at least a factor of 3 to 6 times shorter than any comparable device out there. Several classes of rectifiers were chosen for final development, which means they were the first production GaAs rectifiers. The first, the 180-V/20-A XGR2018CT, is available now in small quantities.



The second rectifier, which has 3- and 8-A versions, is rated at 600 V. The 3-A rectifier, aimed at power-factor correction, will be available in small quantities early next year. The 8-A device, targeted for motor-drive applications, will follow later in the year. Help will be available for potential users of these devices when they reach the market. Prototypes of all three devices have been in the hands of Motorola application engineers for sometime *(see the table)*.

It should be noted that relative to available high-speed silicon rectifiers, the 180-V/20-A GaAs rectifiers won't be inexpensive: The first units from production late this year will cost about $12 each in quantities of 1000. Motorola expects this price to drop approximately 40% once volume production is reached. Motorola's ultimate goal will be to price the rectifier at a level close to that of similarly rated silicon rectifiers. The lower-current 600-V devices will run about $4 each.

SILICON LIMITATIONS

At voltages below 200 V, silicon Schottky diodes do the job quite well. Many power supplies needing higher-voltage rectifiers will employ multiple low-voltage Schottky diodes connected in series rather than fast or "ultra fast" recovery silicon p-n diodes and 200-V silicon Schottky diodes. The ideal high-speed rectifier, regardless of voltage rating, must meet the following requirements at high temperature:

- Provide minimum forward-voltage drop V_f at rated forward current to limit conduction losses.
- Exhibit minimum reverse-leakage current I_r to limit losses when the reverse voltage is applied.
- Recover rapidly (offer minimum reverse-recovery time t_{rr}) to limit switching losses.
- Recover softly to limit EMI, switching losses, and switching stress.

However, above about 200 V, it's no longer practical to connect low-voltage Schottky diodes in series. As a result, a power-supply designer is stuck with using fast and ultra-fast silicon diodes whose performance starts to degrade at that voltage. Moreover, even available 200-V Schottky diodes provide limited performance.

The 180-V XGR2018CT consists of a pair of 180-V, GaAs Schottky-diode rectifiers in a TO-220 package, a standard configuration in which the two devices share a common cathode connected to the tab and the center pin *(Fig. 1a)*. The two isolated anodes connect to the outside pins. Single-diode versions will be available in the SMB package in 1995.

Each Schottky diode in the TO-220 package handles a maximum average rectified forward current (I_f) of 10 A at a junction temperature of 150°C while standing off 180 V of reverse voltage (V_r). The two in parallel handle 20 A. With a V_r of 180 V, maximum instantaneous I_r is 500 μA at 25°C. While passing that 10 A, maximum instantaneous V_f for each diode is just 1 V. Moreover, maximum t_{rr} is 10 ns (at a V_r of 100 V, I_f of 8 A, and a di/dt of 400 A/μs).

Though it's basically a pair of "large" vertical planar Schottky-barrier junctions, the XGR2018CT can be considered an IC because both rectifiers are formed from the same die. That is, current flows from the two anodes on the top of the die to the cathode that's common to both on the bottom *(Fig. 1b)*. The integration not only simplifies packaging, but more importantly, ensures optimum

MOTOROLA'S GaAs SKUNK WORKS

I've been told by Scott Delaney of Motorola that their GaAs rectifiers came about in a program reminiscent of the famed Skunk Works of Kelly Johnson at Lockheed (the source of Gary Power's U2 spy plane, and like these rectifiers, a user of titanium in the Mach-3 SR-71 Blackbird reconnaissance plane). The original concept came from Motorola's Sam Anderson and his research team in 1991. Anderson's team started to make the concept a reality at that time and delivered the first working devices early in 1992. In the pursuit of their vision, the team broke every rule in the book, including working weekends. Anderson and his group also had to endure the innovation-killing "you can't do that" statements.

In late 1992, the company presented Dr. Ali Salih and his product development team with the task of bringing the first GaAs rectifier to market. That is, turn the working rectifier from Anderson's effort into a viable product that would meet the demanding application and production expectations of Motorola's customers. That's when I first heard about it, and decided then it was destined for the cover of *Electronic Design* someday. However, this is the first news of it in print.

Over the past few years, Ali's group faced and overcame many hurdles, both technical and nontechnical. They ranged from packaging issues to production environments, from thermal management and a need for mechanical finite-element analysis to reliability testing and as always cost, cost, cost. I'll attest to that. At one period over the past two years, all evidence of the program disappeared.

Just the differences in material characteristics between silicon and GaAs presented severe technical challenges. GaAs is weaker than silicon, has a lower thermal conductivity, operates at higher temperatures and *is not* desirable in plant drainage systems. Imagine the packaging issues with a power-dissipating die that will run hotter because of lower thermal conductivity. Using normal assembly techniques aren't a given due to die strength and environmental concerns. And even if a package could run hotter, would anyone want a device at 250°C in a potted module?

The team's work isn't finished. For example, they didn't ignore applications. In fact, one of their application engineers, Jim Spangler in Chicago, an expert on power-factor correction, walked me through several applications, finally making clear why customers might pay over $10 for a device that until now typically cost them about a "buck."—*FRANK GOODENOUGH*

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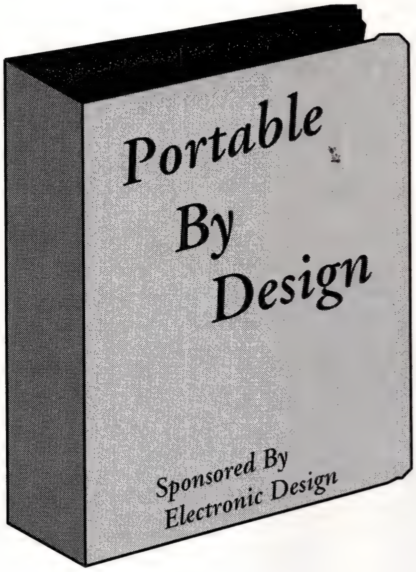

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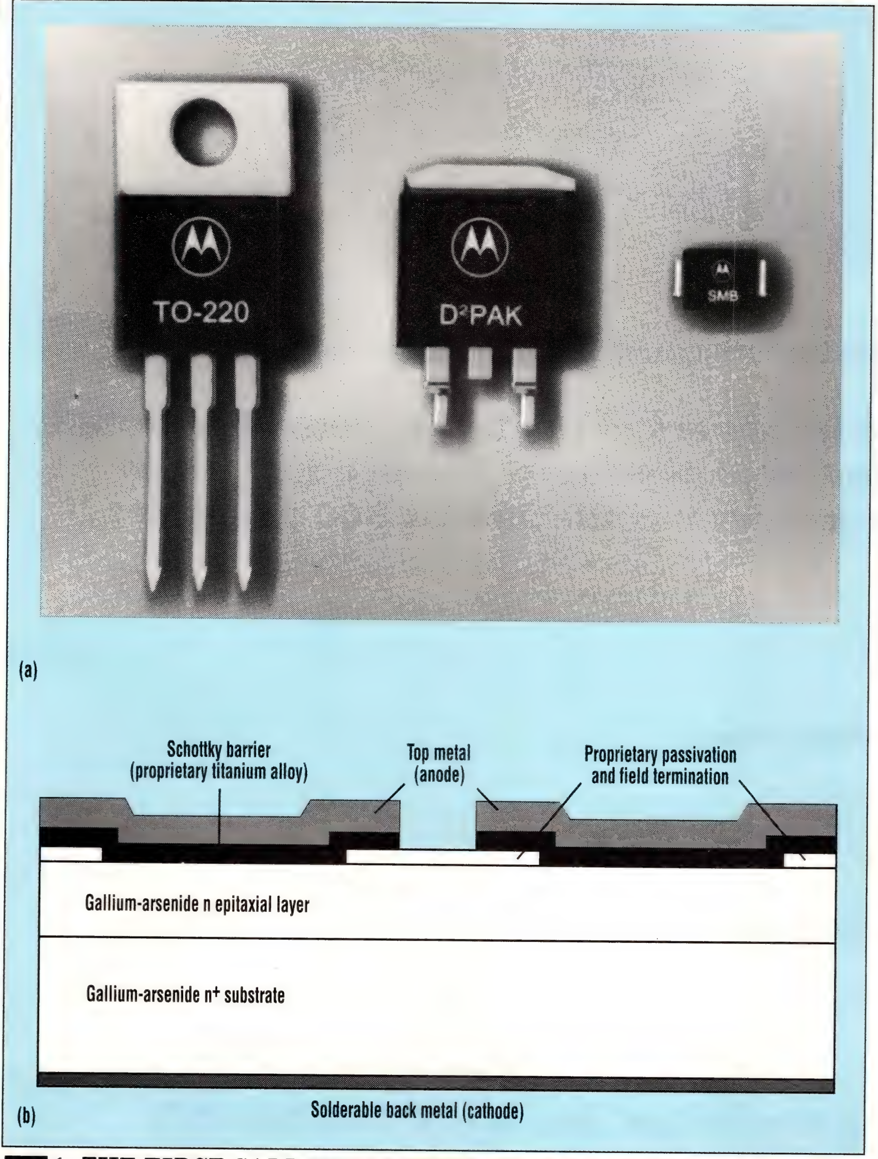
matching between the V_f of the two diodes. The key to the device lies in Motorola's proprietary termination, passivation, and titanium barrier-metal processes.

The 180-V GaAs rectifiers will find homes in high-frequency 48-V-output forward converters for telecommunication systems and modules. In these transformer-based applications, they'll be used as output rectifiers to increase power-supply efficiency by at least 4%. While an improvement of 4% may not sound like much at first, it is significant. Take, for example, a 300-W (regulated output) 2-by-4-in. switcher module running at 90% efficiency, which means the package and the devices in it can dissipate 30 W. Increase the switcher's efficiency to 94% and theoretically the same module can now be rated at 500 W, because 6% losses result in the same 30-W dissipation.

Why did Motorola choose GaAs, with all of its problems or potential problems, as the material for a family of advanced high-voltage, high-frequency rectifiers? Problems include limited wafer size (the XGR2018CT is built on 2- or 3-in. wafers), wafer fragility, the semi-insulating substrate, the lack of silicon dioxide for all of its tasks, and its poor thermal conductivity. Furthermore, why Schottky diodes?


TO-220
D²PAK
SMB
(a)
Schottky barrier (proprietary titanium alloy)
Top metal (anode)
Proprietary passivation and field termination
Gallium-arsenide n epitaxial layer
Gallium-arsenide n+ substrate
Solderable back metal (cathode)
(b)

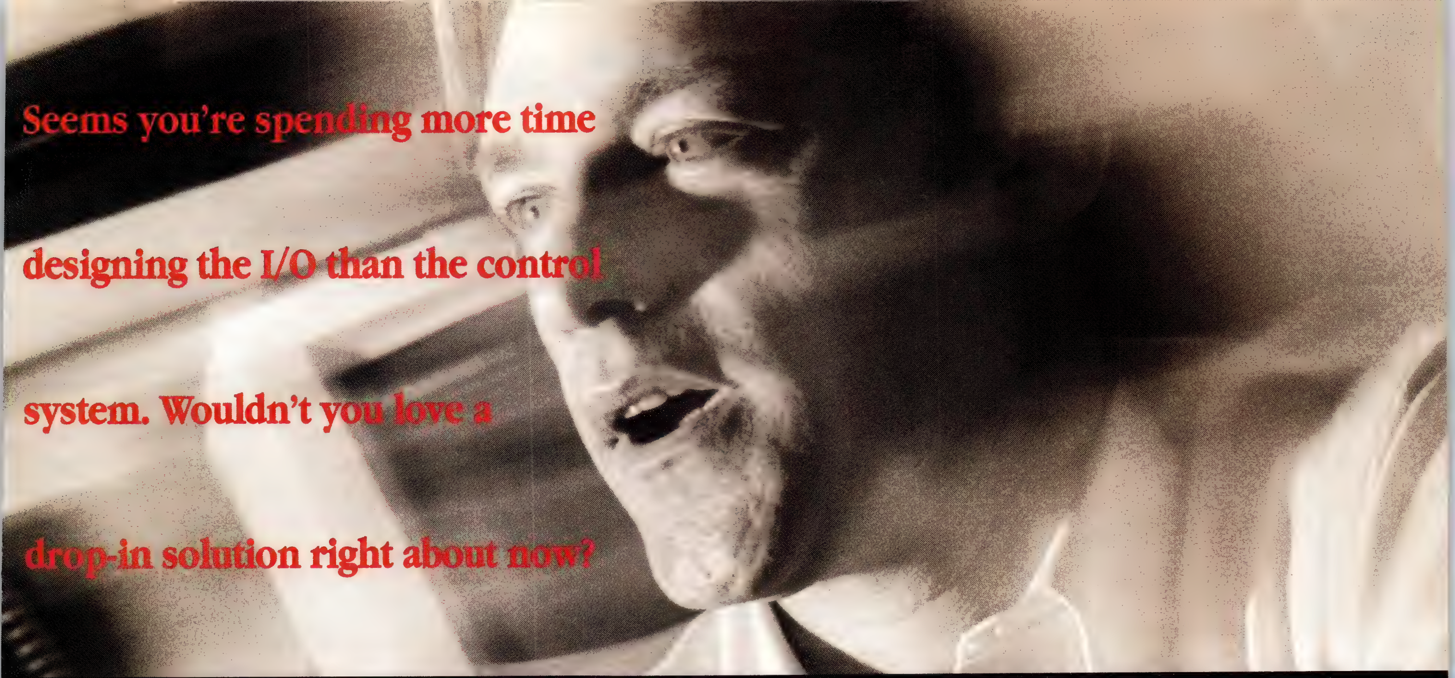
1. THE FIRST GALLIUM-ARSENIDE POWER RECTIFIER to hit the industry is this dual device rated at 180 V and 10 A (per device). It comes in a TO-220 package, and will later be available in D²PAK and SMB packages (a). The device starts with a GaAs substrate and an epitaxial layer. A pair of Schottky-barrier diodes formed from a titanium alloy make contact with the epitaxial layer (b).

For starters, to overcome the physical limits imposed by silicon, a material offering a wider energy bandgap than silicon's 1.11 eV was needed. Of the materials potentially available—GaAs, diamond, and silicon carbide—GaAs appeared more feasible because its crystal-growth and wafer-processing technologies are more mature, although not up to those of silicon. Its larger energy bandgap of 1.42 eV provides three inherent advantages over silicon: higher switching speed, particularly for higher-voltage Schottky diodes; higher temperature operation; and lower leakage current at any temperature. Although silicon devices can operate at temperatures up to 200°C with limited performance, GaAs ICs operate at temperatures up to 350°C with performance equivalent to silicon at 200°C.

The larger energy bandgap does create a higher V_f, but the carrier mobility of GaAs, five times that of silicon, mitigates this effect. At a voltage rating of about 200 V, silicon and GaAs devices show about equal forward-voltage drops. Above 200 V, the V_f of GaAs runs lower, which is fortuitous because 150 V is about the voltage rating at which silicon performance starts to deteriorate. Moreover, Schottky diodes were chosen because they are majority carrier devices. As a result, they don't suffer from minority-carrier injection and its attendant speed-reducing stored charge.

Motorola has spent many years researching and developing GaAs technology. The company has processed the material for optical devices (LEDs) for over two decades and for RF communication devices for ten years.

Motorola calls the first 600-V rectifier (the 3-A device) a "fast/soft" recovery rectifier, and its soon-to-arrive higher-current counterpart a "soft/fast/high-power-density rectifier. The 3-A diode recovers from a peak reverse current of about 1 A in about 12 ns, which is virtually lossless switching. The 8-A unit takes a little longer, just over 25 ns *(Fig. 2)*.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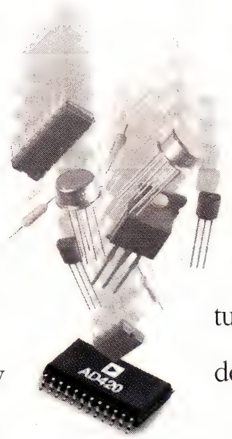

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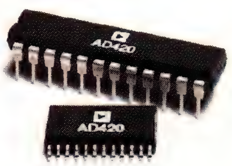

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Typical 600-V ultra-fast silicon rectifiers recover in 30 to 100 ns.

The 3-A rectifier will be used in boost converters, such as in those needed for power-factor correction, while the 8-A rectifier will be employed as a free-wheeling/snubber diode in motor-drive circuits. The 3-A rectifier provides a forward voltage drop similar to that of similarly rated ultra-fast silicon devices (about 2.2 V) while operating at several-fold higher current densities, about 200 A/cm^2. The higher-current 600-V rectifier operates at significantly higher current densities, which isn't a problem in the snubber application. It will potentially change the die and package sizes needed to handle a given power level.

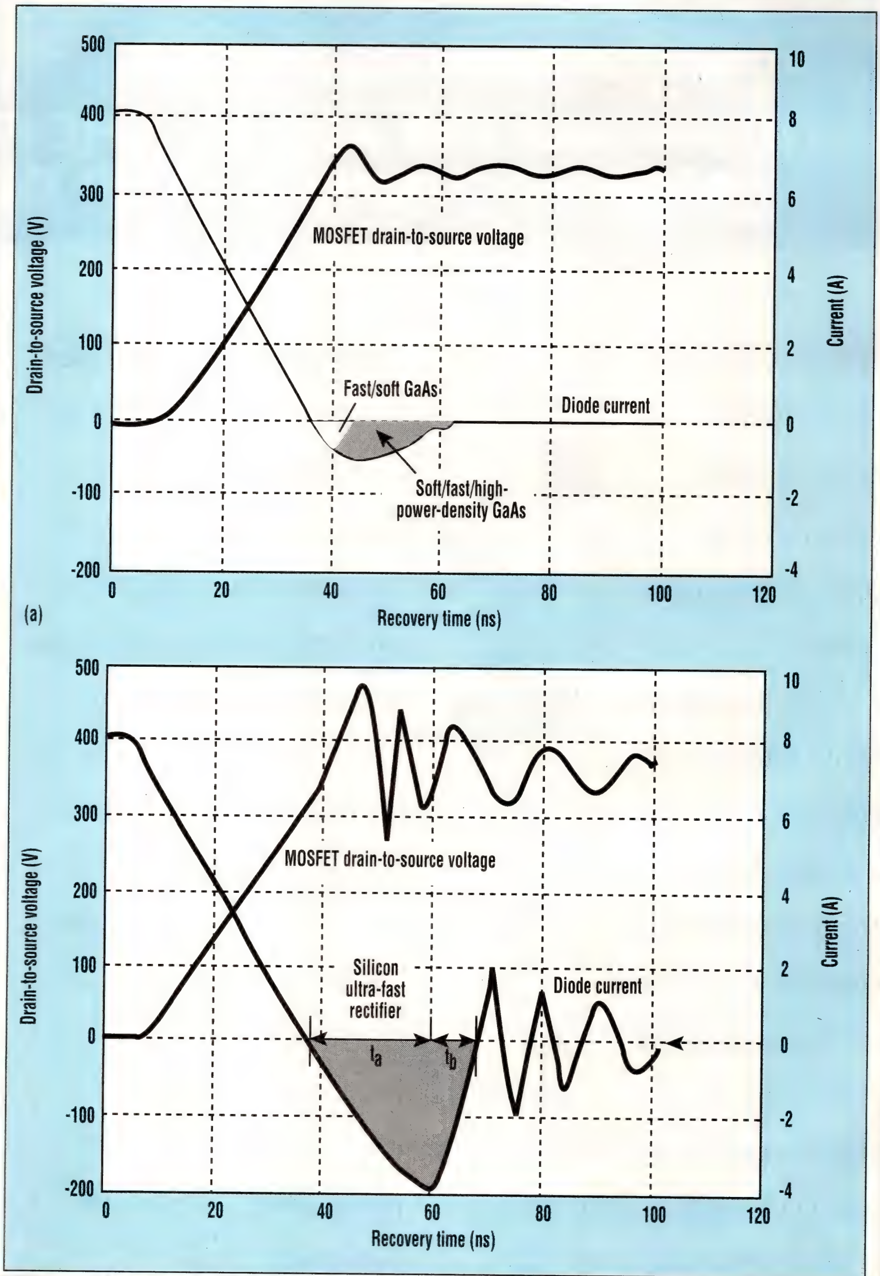
MULTIPLE APPLICATIONS

The 600-V GaAs rectifiers will play an interesting role in many applications. First, their own conduction and switching losses will be lower than those of the best silicon devices for the application. In addition, the GaAs rectifiers can cut losses within power MOSFETs in the switching regulators, producing the high-frequency voltages that GaAs devices must rectify.

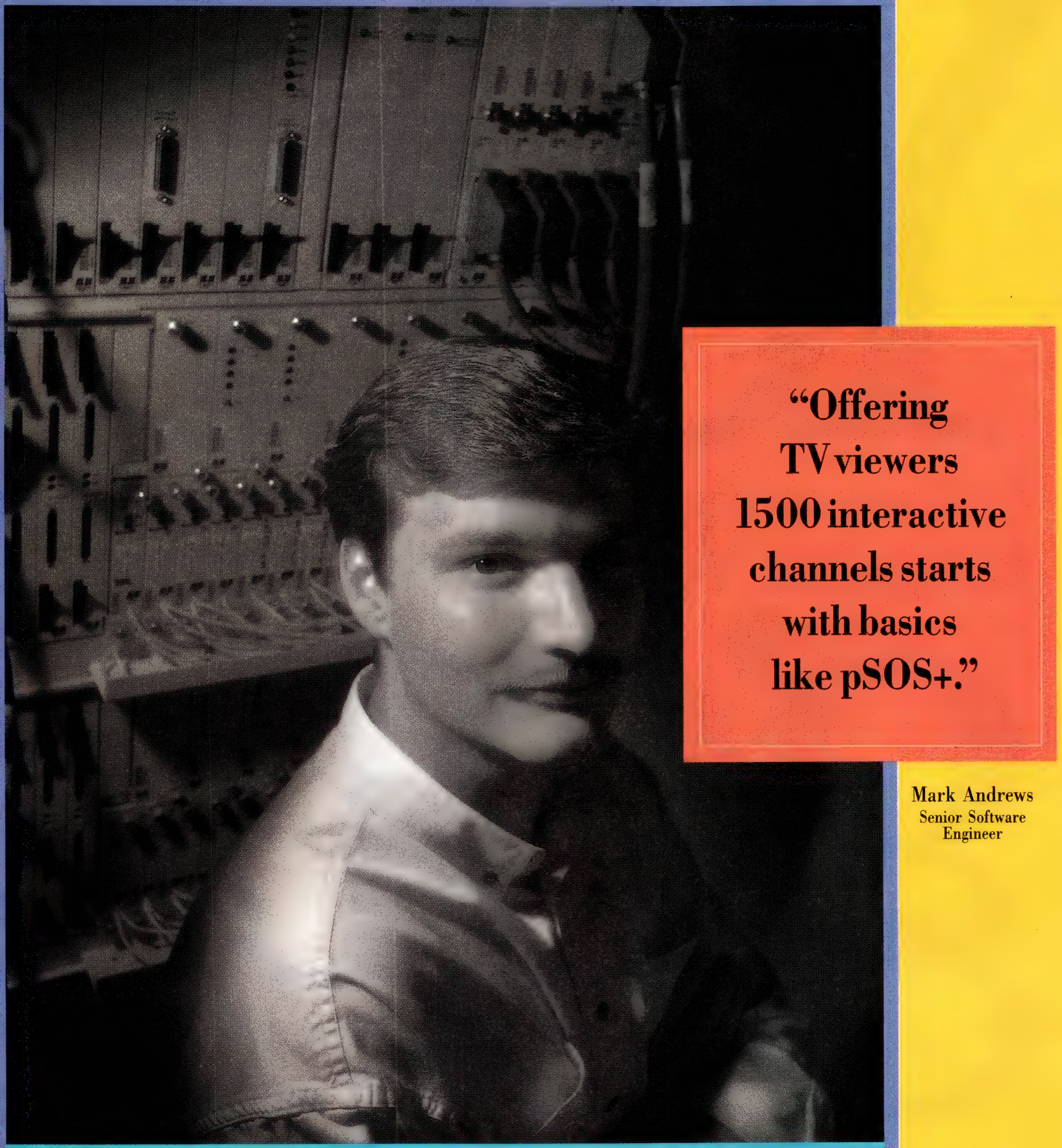
Acting as a free-wheeling diode that drives motors, the GaAs rectifier will provide lower conduction losses thanks to the lower forward drop and lower switching losses caused by the soft recovery. In snubber applications driving inductive loads such as solenoids, switching losses will drop due to the high speed and soft recovery. Moreover, the GaAs rectifier may very well wind up being used in pulse-width-modulated (PWM) switching frequencies as low as 100 kHz. That's because MOSFETs contain an integral parallel diode, unlike the typically-used insulated-gate bipolar transistor (IGBT). Therefore, in snubber-type applications using IGBTs whose switching speeds are approaching 100 kHz, the GaAs Schottky diode may become useful.

The first 600-V device will be particularly useful in power-factor-correction switchers employing a boost topology, particularly those that operate in the so-called continuous-duty mode *(Fig. 3)*. The result will be maximum performance and efficiency in minimum space. In this mode, current flows through the inductor at all times regardless of the duty cycle—although it's usually greater than 50%. Put another way, if running in a continuous-duty mode, the current doesn't go to zero at the end of each cycle. The technique lowers switching noise, reducing both EMI and the size of the EMI filter. In addition, it shrinks down the converter's filter capacitor at the output of the diode.

Continuous mode operation at frequencies above several hundred kilohertz offers many advantages in applications such as power-factor correction. It also has several disadvantages, but these are fixable with these GaAs rectifiers. Here's the problem: Assume a 3-A circuit is using a typical 8-A/600-V ultra-fast silicon rectifier. During the rectifier's reverse recovery time, its reverse current also flows in the MOSFET Q and reaches a peak of –4 A *(Fig. 2, again)*. Moreover, during this period



2. A COMPLETE SOFT RECOVERY is provided by a Motorola 600-V fast/soft GaAs rectifier in a speedy 5 ns, virtually unmeasurable in production runs (a). In a similar circuit, a 600-V silicon ultra-fast rectifier takes 30 ns (b).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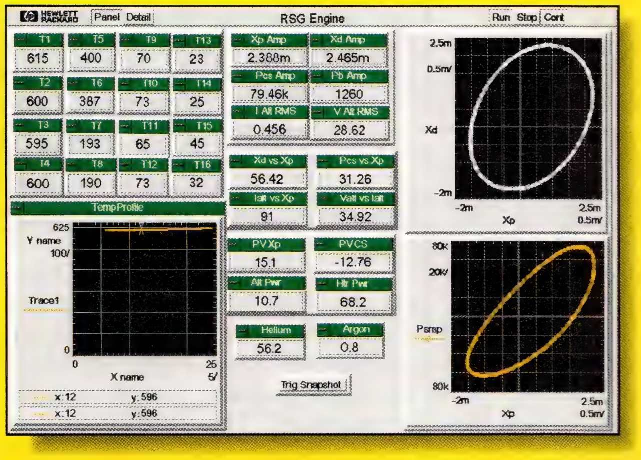

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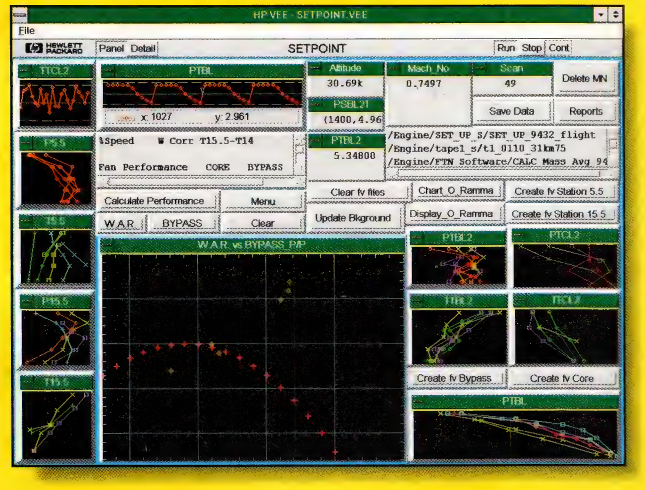

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COMPARISON OF MOTOROLA'S GaAs SCHOTTKY DIODE RECTIFIERS

Application	Part #	Rating	Package	Semiconductor platform
(1) 48-V output dc-dc converters	XGR2018CT	20 A/180 V	TO-220 (now) D^2 PAK ('95)	180-V GaAs; current density = 200 A/cm^2
(2) PFC/snubber	not available	3 A/600 V	SMB ('95)	600-V, fastest GaAs (10 ns t_{rr}); current density = 200 A/cm^2
(3) PFC/motor drive (die size similar to #2)	not available	8 A/600 V	TO-220 ('95) D^2 PAK ('95)	600-V GaAs (25 ns t_{rr}); > 200 A/cm^2

the FET is no longer in saturation with minimum voltage between drain and source (V_{DS}). Rather, V_{DS} climbs to the input voltage (400 V as shown in the figure) and then rings even higher. In addition, the rectifier's reverse-recovery current also rings.

The FET's power dissipation, the product of V_{DS} and rectifier reverse current, reaches a peak value of 800 W for 20 ns, and an average value of greater than 400 W for over 60 ns, severely stressing the FET and significantly upping the dissipation of the supply. Handling the problem requires a higher-power/higher-voltage FET and a larger heat sink. The FET must be rated for both higher power to handle the increased dissipation and higher voltage to handle the ringing transient. The higher-voltage FET in turn has greater forward conduction losses, further increasing power dissipation.

NO VISIBLE RINGING

Replacing the silicon ultra-fast rectifier with the fast/soft 600-V GaAs rectifier changes the playing field. Due to the Schottky diode's minimum stored charge, it recovers completely in 5 to 10 ns with no visible ringing *(Fig. 2a, again)*. Peak reverse current is under 1 A and average current during recovery is less than 0.5 A. The FET's V_{DS} peaks at a little over 350 V and settles quickly to about 325 V with minimum ringing. Consequently, the average power dissipation during reverse recovery runs under 130 W, which is a far cry from the 400 W if a silicon rectifier was used.

Motorola's application engineers ran a comparison test between similarly rated 600-V silicon and GaAs rectifiers while the devices were operating in a continuous-mode boost converter. The following results indicate the advantages of using GaAs rectifiers:

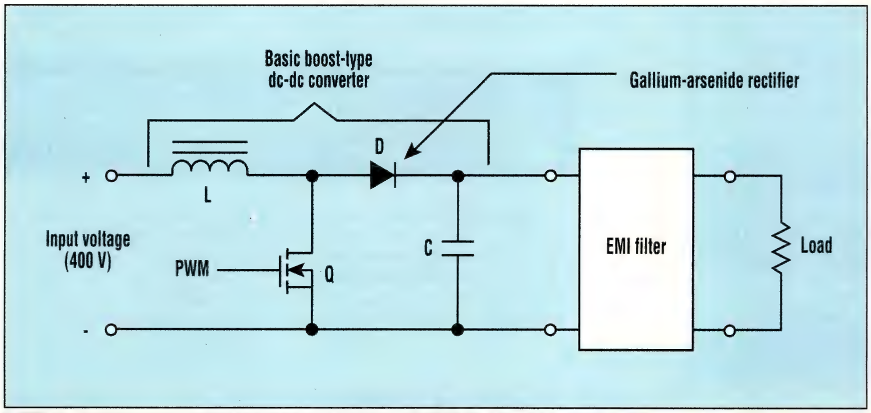
- Over a 40% reduction in power loss
- 20°C lower heat-sink temperature for both the rectifier and MOSFET
- 80% reduction of the MOSFET's overshoot
- Significant reduction in total harmonic distortion and thus EMI

As a result of this test, the frequency range of the continuous-mode technique is expected to be raised from the 100 kHz possible with silicon rectifiers to above 500 kHz using GaAs ICs—significantly reducing the size of the passive devices and increasing the power density.

The low-forward-drop rectifier, in a similar but higher-current application, recovers in under 25 ns—and maximum reverse current peaks at about 1 A. The FET's V_{DS} rings somewhat but settles out quickly to about 325 V. As a result, the average power dissipation in the FET for 25 ns is now less than 100 W.

The strength of these rectifiers lies in their speedy recovery, but if that recovery wasn't as soft as has been demonstrated, their applications would be limited. The reason is that if the diodes recover too fast, the rectifiers will generate harmonics much like the MOSFETs' ringing, which becomes a severe source of EMI. However, not only are these devices faster than their silicon equivalents (as well as exhibit limited reverse current), but their recovery is softer than the silicon devices.

Soft recovery is best defined by a figure of merit, T_b/T_a, or di/dt of I_b divided by di/dt of I_a. T_a and T_b are the periods of time when the reverse current is increasing and decreasing, respectively. The derivatives indicate the slopes of the reverse-recovery current versus time during the respective periods *(Fig. 2b, again)*. The higher the figure of merit, the softer the recovery—regardless of what the actual recovery time is. It's usually less than 1 for silicon rectifiers and from 1 to 5 for GaAs rectifiers. The 180-V devices show a figure of merit of about 1 or 2, and the new 600-V rectifiers show a figure of merit of about 4 or 5.☐



3. THE CONTINUOUS-MODE OPERATING FREQUENCY of a boost-topology switcher can be upped from 100 kHz to as high as 500 kHz by using a GaAs rectifier, thereby increasing the unit's efficiency.

PRICE AND AVAILABILITY

The 20-A, 180-V XR2018CT GaAs rectifier goes for $12 each in lots of 1000. Small quantities are available from stock.

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15th Aerospace Testing Seminar, Oct. 11-13. Radisson Plaza Hotel, Los Angeles, CA. Contact Julie Kendrick, The Institute of Environmental Sciences, 940 E. Northwest Highway, Mount Prospect, IL 60056; (708) 255-1561; fax (708) 255-1699.

Singapore Informatics '94, Oct. 13-16. Singapore World Trade Center, Singapore. Contact Ellen Wong, Commerce Tours International, Inc., 870 Market St., Suite 920, San Francisco, CA 94102; (415) 433-3072; fax (415) 433-2820.

2nd ACM International Conference on Multimedia (ACM Multimedia '94), Oct. 15-20. Hyatt at Embarcadero, San Francisco, CA. Contact, John Limb, Hewlett-Packard Co., 1501 Page Mill Rd., M/S IU-19, Palo Alto, CA 94304; (415) 857-2255; E-mail:jol@hpl.hp.com.

1994 IEEE GaAs IC Symposium, Oct. 16-19. Wyndham Franklin Plaza Hotel, Philadelphia, PA. Contact Donald C. D'Avanzo, Hewlett-Packard Co., 1412 Fountaingrove Pkwy., Santa Rosa, CA 95403; (707) 577-2644; fax (707) 577-2036.

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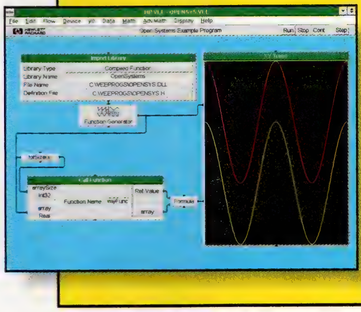

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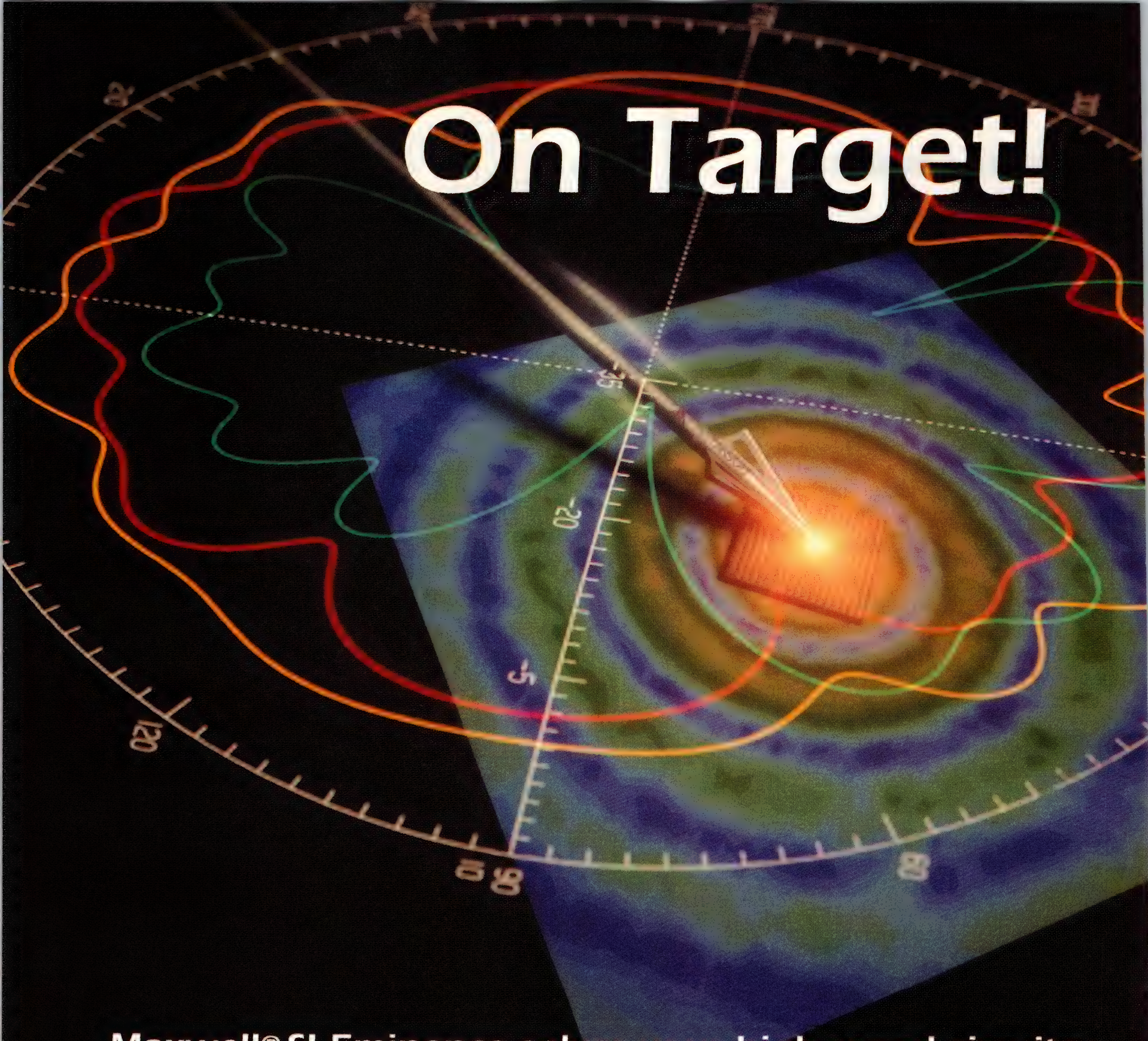

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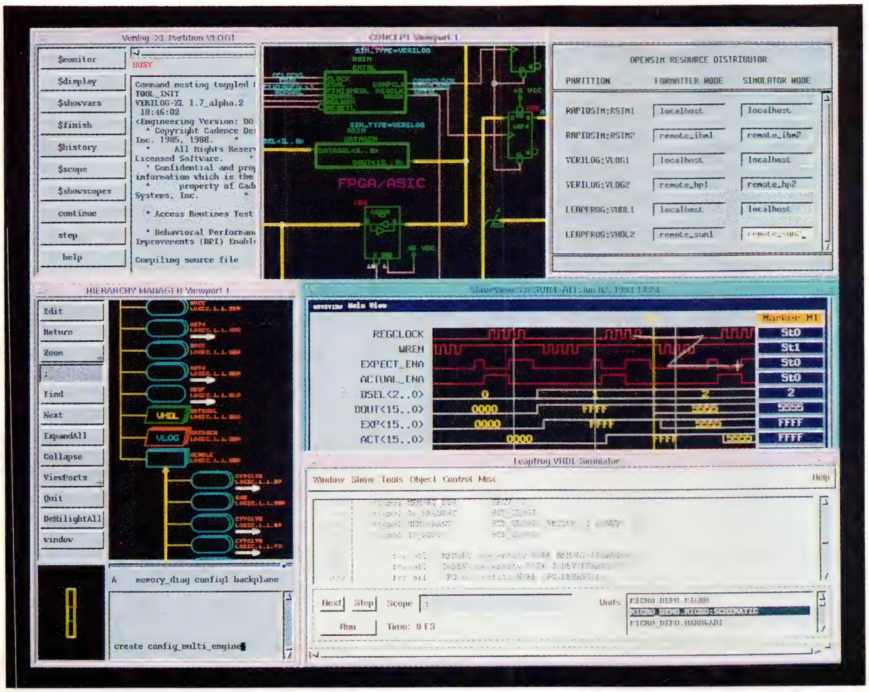

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		Marker M1
REGCLOCK		St0
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EXPECT_ENA		St0
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EXP<15..0>	0000 FFFF 5555	FFFF
ACT<15..0>	0000 FFFF 5555	FFFF

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BACKPLANES MESH SIMULATORS INTO ONE ENVIRONMENT

LISA MALINIAK

SIMULATION BACKPLANES AID SYSTEM DESIGN, BUT MAY COST ENGINEERS SPEED AND EASE-OF-USE.

The 1994 *Electronic Design* EDA survey mailed to a random group of electronic-design-automation users showed, among other things, that engineers would like to simulate more of their designs. But because no one simulator addresses all modeling and performance issues, system verification usually requires co-simulation with multiple tools. Engineers are then faced with the difficult task of integrating the simulation tools—making them work together smoothly in one environment. A new type of EDA software technology, called a simulation backplane, proposes to ease the integration issues associated with co-simulation.

Actually, there are many reasons why engineering teams use multi-simulator environments. First of all, most designs consist of many different technologies that require multiple models and simulators. Engineering organizations want to protect their investment in models, and the requirements for these various models often drive the need for co-simulation.

Also, because engineers want to use the best tool for each task, system design may involve several design-verification products. Finally, inter-group and inter-company design projects are common. Co-simulation provides a reliable way for each group or company to create systems using the tools they're most effective with, yet assemble and verify all of the modules when necessary.

Basically, a backplane lets a number of simulation engines be combined into one simulation session. It's a unified environment that supports partitioning and synchronization for every integrated simulator. It must have an open architecture to facilitate integration of additional third-party and custom simulators or tools. In addition, a backplane should support distributed simulation over multiple processors or workstations. And it should unify a multiprocessing environment with a common interface *(see "Simulation back-*

planes need front panels," right).

As with any emerging technology, the gain brought about by simulation backplanes comes at a cost. Engineers using backplanes face increased overhead (meaning longer run times) due to the communication between engines. In addition, backplanes generally aren't easy to use. For example, simulator integration and design partitioning among the simulators can complicate backplane usage. Potential backplane users must make a trade-off between the extra time and effort required versus the security brought about by a full system verification.

Because of those trade-offs, engineers using just two simulators in a design may want to consider directly coupling the tools. For example, engineers that need to simulate a system design with both VHDL and Verilog hardware-description-language models might consider direct-coupling and other options in addition to using simulation backplanes *(see "Verilog-VHDL interoperability," p. 62).*

IT'S NOT A FRAMEWORK

While backplanes may sound similar to frameworks, they're not the same thing. A framework can be used to tie simulators together in a static, rather than dynamic, fashion. More specifically, a framework can help generate input stimuli for each simulator, and also bring waveform data back from the simulators into the framework environment. The framework is limited, however, to running the simulations serially, finishing one simulation first before doing another. An ordinary framework can't let two or more simulators dynamically interact.

Simulation backplanes, on the other hand, allow the integrated simulators to run in parallel and interact dynamically, and that's not an easy accomplishment for many reasons. Consider the simple example of a digital logic representation that flows from a gate into a transistor. That event requires the backplane (connecting digital and analog simulators) to map a state or an event-driven algorithm into a simulator that solves the differential equations used to characterize analog devices.

SIMULATION BACKPLANES NEED FRONT PANELS

Simply put, simulator backplanes are a necessary evil. Although they impose a significant performance penalty, backplanes are currently the only way for engineers to combine such disparate domains as VHDL or Verilog models, hardware-accelerated gates, and analog blocks in one simulation.

But backplanes only address part of the problem. Linking two or more simulator kernels together solves only the data-generation problem. In other words, engineers can use multiple simulators tied together through a backplane to generate results with the appropriate accuracy level for each part of the design. However, backplanes rarely do anything to alleviate the interpretation problem, which means understanding all of the data to make effective design decisions.

Many backplanes force engineers to use a different user interface (UI) for each simulator kernel, both for simulator control and data analysis. The overhead tasks of setting up the signal-trace lists, initializing and synchronizing the simulators, and cross-referencing results between two or more trace-file displays force users to spend far more time running the tools than understanding and fixing their design.

The best way to interpret the simulation data is to create a front panel for the backplane. This front panel would integrate all of the simulators running in the backplane. It provides a single interface to control the kernels, which speeds learning to use the combined toolset and prevents the inevitable confusion that arises when using incompatible simulator-command sets.

A front panel also would combine each simulator's trace-file output into a coherent, unified display. Not only does this provide the same benefit of a single command set, but more important, it eliminates the domain-specific view problem. Most backplanes today display data in the domain in which it was calculated—analog data is shown in an analog display, digital data in a digital display, and so on. This is acceptable for some designs, but not in many multi-simulator environments.

Engineers are on their own when they want to compare data in different domains, or want to use a common format when tracing drivers of signals that span domains. They are then forced to jump back and forth between simulators, estimating transition times, scribbling calculations on a sheet of paper, and other manual tasks. This problem is particularly important with simulation backplanes because the interface between domains is exactly where automation is needed. In fact, the hassles associated with debugging an interface are probably what encouraged engineers to use a simulation backplane in the first place.

Ultimately, the front panel could make simulating multiple domains together as easy as simulating a single domain—the front panel would automatically select the appropriate simulator kernels and allow users to display their data in virtually any form. Several tools today are working toward that type of a front panel. For example, Redwood Design Automation's Reveal interactor software unifies data from different tools, and many vendors' waveform displays support both analog and digital views. While the products are taking the first step toward interpreting multiple forms of data, it's the advent of front-panel products that will allow engineers to realize the full potential of simulation backplanes.

Contributed by Jeff Lewis, director of product marketing for Redwood Design Automation, San Jose, Calif. (Redwood has signed a letter of intent to merge with the Alta Group of Cadence Design Systems Inc., Foster City, Calif.)

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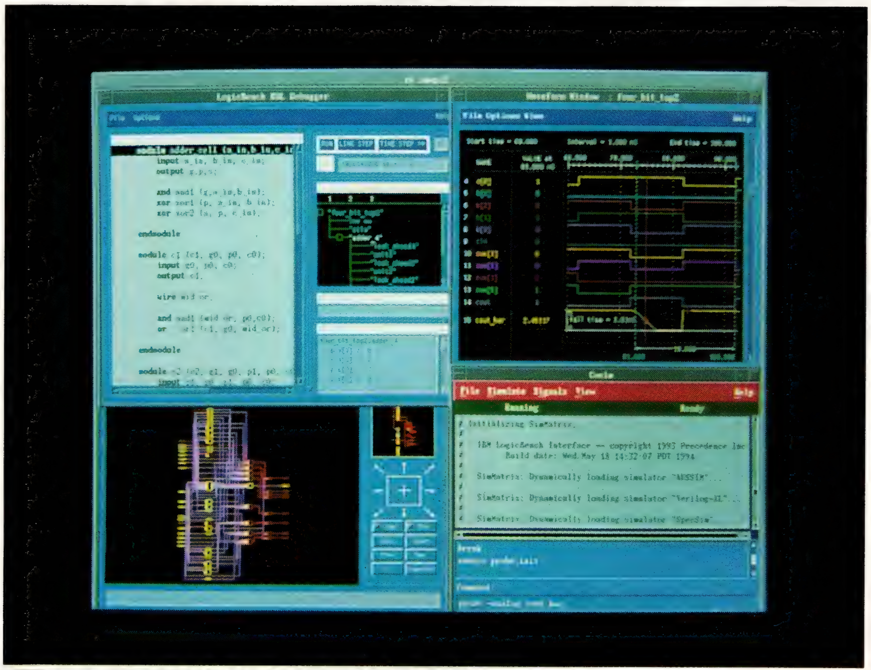

1. A CO-SIMULATION WINDOW IN THE bottom-right corner shows the Precedence SimMatrix backplane at work within IBM's LogicBench design environment. The backplane activates three different simulators (the AUSSIM mixed-level simulator, the SPECSIM switch-level simulator, and Verilog-XL), which are integrated into one seamless environment.

The backplane has to represent the gate in the digital simulator, represent the transistor in the analog simulator, and establish some way of getting information back and forth between the two.

An interface model that maps the digital output to an analog input is a critical part of simulation-backplane technology. The method used to map the digital 0 or 1 states into analog voltage representations (and vice versa) profoundly affects the accuracy of the backplane and the simulation performance. A backplane containing a built-in model for mapping information and a flexible user-defined model will make the complicated nature of a multi-simulator environment more straightforward to use.

MAPPING STATES

Communication between analog and logic simulators isn't the only complex problem that faces simulation backplanes. A backplane may have to map state information from one logic simulator into another. And logic simulators can be very different. Some may have six states and others have 28. Many have an infinite number of states.

Co-simulation requires technology to partition a design among several simulators. A partitioner might generate multiple net lists and interface models that represent the entire design. Then, the partitioned design is input to the backplane. During the co-simulation process, all of the simulators will generate outputs. The backplane should be able to collate the outputs into one representation for analysis.

The dynamic link between simulators is a critical part of the backplane technology. Every simulator has a different way of scheduling events. For two simulators to function together in one environment, the time queues must be synchronized. One way to handle this timing issue is to make a backplane with its own synchronization engine. The time queues of the simulators in the backplane become slaves to the synchronization engine, which controls event queuing and timing in each simulator.

Several simulation backplanes currently exist on the market. Most involved in the technology is Precedence Inc., Santa Clara, Calif., which was founded in 1991 specifically to fill the need for a multi-simulation environment. The company's proprietary SimMatrix simulation backplane manages the flow of information between simulation engines, and orchestrates synchronization between the multiple simulation algorithms.

The front-end environments supported by SimMatrix include those from Cadence Design Systems, Mentor Graphics Corp., and Viewlogic Systems. SimMatrix preserves the functionality of these environments while enabling co-simulation using additional design-verification tools from various EDA vendors. The graphical and textual user interface and debugging environment of each simulator is preserved and available to users.

Precedence also offers SimMatrix Integration Toolkits. These are designed for users with proprietary simulators, or vendors of commercial simulators who wish to integrate into the SimMatrix backplane. The foundation toolkit is based on the Precedence Procedural Interface (PPI), and provides automatic circuit partitioning, hierarchical net-list generation, networking or multiprocessing, and extensive debugging and test-bed facilities. In addition, the company offers integration consulting services to assist with individual user requirements.

CERTIFICATION PROGRAM

An industry-wide simulator interoperability program was announced by Precedence at the Design Automation Conference in June. The SimMatrix Gold interoperability criteria and certification help engineers make informed choices about multi-simulator solutions. SimMatrix Gold Certified solutions guarantee a consistent feature set that brings the benefits of interoperability. This feature set contains test installation, user interface, design partitioning, synchronization, run-time features, and report and error handling.

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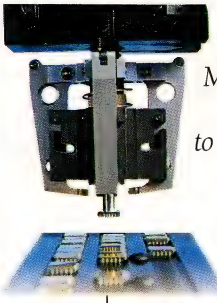

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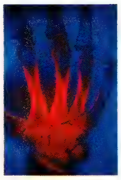

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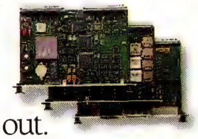

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IBM recently adopted the Precedence simulation backplane for both internal IBM use and as part of the IBM commercial EDA environment sold through the company's Altium subsidiary, Charlotte, N.C. The IBM LogicBench design environment, with SimMatrix co-simulation, enables IBM design groups and Altium customers to combine simulation algorithms from commercial and proprietary IBM technology *(Fig. 1)*. This technology includes IBM's AUSSIM VHDL simulator, cycle-based simulators, circuit-level analog simulators, and the Verilog simulator.

PRESERVING INVESTMENTS

With the multi-simulator backplane, both external and internal engineers can preserve their investment in existing simulation tools and libraries. It also alleviates the model-availability problem, promotes design reuse, and facilitates large designs that include elements from several design groups with a variety of tools. Dr. John Darringer, director of the EDA Laboratories for IBM Microelectronics, Poughkeepsie, N.Y., explains that the company's customers need interoperability with their current Verilog and VHDL tools. The SimMatrix backplane lets IBM create a mixed-language, mixed-mode, and mixed-level system-verification design environment.

Another company exploiting the Precedence SimMatrix backplane is Epic Design Technology Inc., Santa Clara, Calif. Epic uses the backplane in its Vertue co-simulation software. Vertue links the company's TimeMill and PowerMill timing- and power-simulation tools with Verilog for mixed-level simulation of IC designs. The backplane provides a transparent interface between the simulators, and allows one or more transistor-level components to simulate directly with Verilog as if it were modeled in the Verilog hardware description language. The Vertue interface also includes partitioning, net-list generation, state and strength mapping, synchronization, and debugging.

The SimBus simulation backplane developed by Viewlogic Systems Inc., Marlboro, Mass., also is built on the Precedence technology. SimBus integrates point tools into one simulation environment, thus combining all of the tools' capabilities. There are four main SimBus simulation-backplane elements: communication, partitioning, synchronization, and user interface.

Communication must be flexible, so SimBus supports three different communication mechanisms. These are shared-memory semaphores for fast performance within one machine, Unix sockets for Ethernet environments, and multi-threaded, multi-processing capability for parallel-computing architectures.

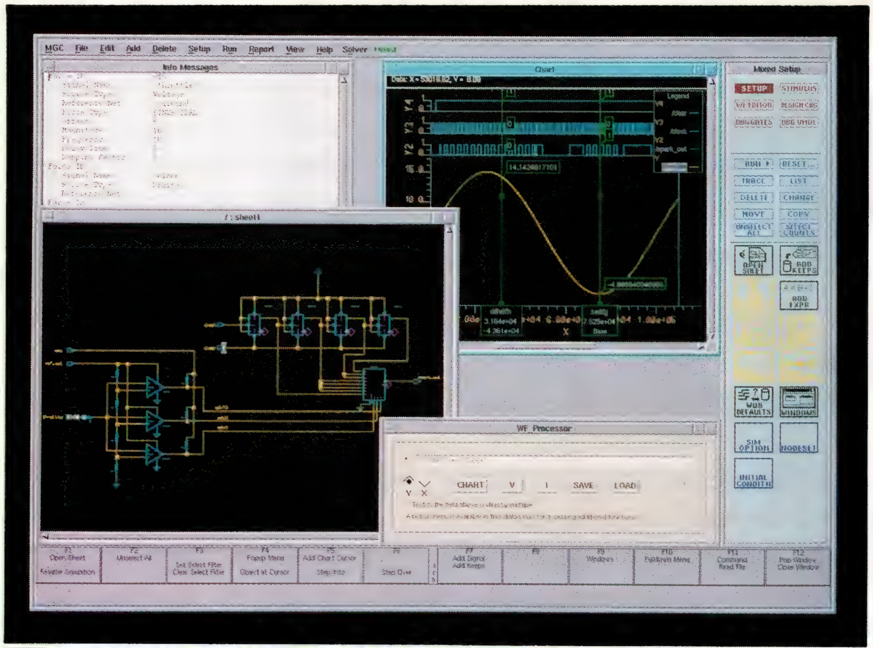
Because partitioning must be accurate and user-friendly, SimBus lets users define design partitions either using language-based commands or graphically with a schematic-capture tool. Users have complete control over the partitioning of their design.

Timing synchronization can be a major source of errors and performance problems in simulation integration. In fact, synchronization errors often require costly time reversals that can degrade speed by orders of magnitude. SimBus uses IEEE VHDL timing models and an innovative double-conversion approach to ensure accuracy and efficiency in each integration.

The SimBus user interface combines a common control interface and a waveform processor. In addition, engineers can continue to utilize the user interface and development environment of each of the integrated simulators.

MODULAR BACKPLANE

OpenSim is a simulation backplane created by Cadence Design Systems Inc., San Jose, Calif. It consists of three modules—Simulation Executive, Partitioner, and Synchronizer. The Simulation Executive controls the backplane process and communication with the user environment through the company's Communications Manager. It takes interactive commands and messages from other tools in the system, and then dispatches instructions to any other tool listening in the system. This includes commands for environment setup, design partitioning, user interactive stimulus, and various types



2. THE CONTINUUM MIXED-SIGNAL SIMULATOR designed by Mentor Graphics joins analog and digital engines through the company's FlexSim simulation backplane. With the backplane, the two engines are brought together as one simulator with a common user interface.

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of debug operations.

The Partitioner module automatically divides the design among the various simulators in the backplane. Engineers use the company's Hierarchy Manager to graphically partition the design based on computing resources, design size, model availability, and design phase. During pre- and post-layout system-level simulation, the Partitioner automatically takes standard-delay format (SDF) back-annotation data and distributes the SDF delay information to the integrated simulators.

At simulation time, the Synchronizer orchestrates the activities of the integrated simulators, and propagates results among them. Integrated simulators link into the backplane in one of two ways: in the same process for highest performance, or spawned through multi-process interprocess communication for maximum flexibility. Integrated simulators are invoked in one of two ways: using local synchronization for highest performance, or distributed synchronization for increased capacity and performance by leveraging computing resources available on the network.

Mentor Graphics Corp., Wilsonville, Ore., unveiled their FlexSim backplane technology just before the Design Automation Conference. FlexSim tries to balance performance and openness, and is Mentor's second generation of commercial simulator backplanes.

USER INTERFACE

FlexSim incorporates SimView, a user interface designed to front an assortment of simulation algorithms. SimView ties together multiple algorithms and presents them to users as one tool. SimView is shipping as the front end for analog, gate-level, VHDL, Verilog, and hardware-accelerator simulation algorithms. It provides users with consistent design viewing, commands, and results displayed across the board.

The core of the FlexSim backplane technology already supports Mentor's Continuum mixed analog-digital simulation environment, as well as a number of other products *(Fig. 2)*. Third-party simulation kernels can be integrated with FlexSim through the company's OpenDoor program. FlexSim presents two documented application programming interfaces (APIs) to the integrator. One handles synchronization and user-interface control, while the other connects to the FlexSim Design Partitioner.

While these backplane products find uses in many types of simulation environments, some EDA vendors feel that direct coupling of multiple simulation engines is the most efficient solution. With a direct-integration setup, users have no choice of simulation engines—they must use the technology offered by the company. Direct coupling of multiple simulators is tighter and runs faster, but takes more work than a backplane integration.

When creating its mixed-signal simulator, AT&T Design Automation, Murray Hill, N.J., opted to go with a single-core, rather than backplane-based, architecture. Prasad Subramaniam, AT&T's CAE product manager, points to the benefits of the single-core approach. Computer resources are used efficiently because a single process requires less

VERILOG-VHDL INTEROPERABILITY

By most accounts, the hardware-description-language (HDL) "war" is over, and both Verilog HDL and VHDL have been declared winners. As a result, users can select the language that best meets their needs and rest assured that their choice will be a safe one for many years to come. However, with a bilingual world comes a greater likelihood that companies or groups using one language will need to exchange design data with groups using the other, or will want to leverage the strength of both HDLs. Hence, there's a strong need for efficient interoperability between the two languages.

The issues involved in interoperability, though similar to multi-simulation issues, are generally confined to two language-based simulators, and thus present the potential for a different approach than a backplane strategy. The challenge is to develop efficient, performance-oriented Verilog-VHDL interoperability that:

- doesn't require the purchase, knowledge, or use of multiple simulators.
- allows engineers to remain in their native language environment (not have to learn the nuances of the other language), including debug.
- incurs no performance penalty that may limit other multi-simulation strategies.

Cadence Design Systems addressed those language-interoperability requirements by using an interlocking-kernel technique whereby the Verilog and VHDL engines can schedule events directly on the other's event queue. This is only possible through access to the core engines of the two HDL-based simulators (in Cadence's case, the Verilog-XL and Leapfrog VHDL tools). As a result, the company was able to address ease-of-use, functionality, and performance.

Both of the company's simulators offer a feature called Model Import that provides Verilog or VHDL users transparent access to models described in the other language. Basically, three scenarios exist in which language interoperability is required:

1. A VHDL-based design environment that must access Verilog models (e.g., needing access to a certified Verilog ASIC model).
2. A Verilog-based design environment that must access VHDL models (e.g., many CPUs are available only as VHDL models).
3. Both languages are used in their areas of strength by different members of a project team (e.g., using VHDL at the behavioral level and Verilog at the gate level).

Two types of usage are typical with Leapfrog's Verilog Model Import feature. In the first one, memory and disk space, one time queue eliminates synchronization issues, and highly interacting analog-digital circuits are handled more effectively. In addition, a common interface and database simplify operation.

FrontLine Design Automation Inc., San Jose, Calif., created their three-engine Verilog simulation environment without a backplane. The company built a modular system that tightly couples the engines as well as leaves room for additional engine integration. The FrontLine environment uses a piece of software called DriveLine to synchronize the various simulation engines. DriveLine also serves as the mechanism by which the simulation data structures are accessed by the other components of the simulation environment.

While DriveLine's first function is similar to that of a simulation backplane, there are several key differences. Unlike simulation backplanes that incorporate multiple processes in a socket-based implementation, DriveLine is a single process. That means DriveLine is faster because its cuts out interprocess communication. Also, backplanes are designed to integrate all kinds of simulators, ranging from digital to analog, and high-level designs to gates. DriveLine is exclusively for language-based design. Finally, backplanes create complete simulation environments from multiple sources, while DriveLine is meant to incorporate only core engines.☐

HOW VALUABLE?	**CIRCLE**
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

the user incrementally synthesizes Verilog gate-level net lists from the VHDL model input. A logic-synthesis tool is used to incrementally synthesize portions of a large design into Verilog net lists. The user then verifies the accuracy of the synthesis output by co-simulating regression tests using the remaining un-synthesized VHDL design with Verilog gate-level net lists. This design flow is generally employed to leverage the certified Verilog ASIC models. Verilog use within this process is hidden, and users need little or no knowledge of the Verilog HDL. Thus, the VHDL debugger displays and manipulates the synthesized Verilog net lists as if it were a VHDL net list. Furthermore, no performance degradation occurs through the VHDL-Verilog interaction.

With the second type of Verilog Model Import usage, the VHDL designer prefers to use an existing Verilog model as an element of a VHDL design. This is common in large organizations that have pockets of both Verilog and VHDL usage, or where a design team is transitioning from one HDL to another. The engineer in this case employs an existing Verilog design as an element in their VHDL design or test bench, and treats the Verilog model as relatively fixed. The engineer isn't required to know how Verilog works, but the Leapfrog VHDL simulator provides full visibility into the model to display important data that may be known to exist within the model.

Of primary importance to potential users of Verilog-XL's VHDL Model Import feature is the ability to use externally provided VHDL models as part of a Verilog simulation. In this situation, users generally won't be knowledgeable of VHDL.

The VHDL models typically will be large, fairly high-level models of components (such as CPUs). The purpose of the simulation is to verify the Verilog design's behavior within the context of a larger system.

The VHDL models are treated as library modules, and will change infrequently. Verilog models are the elements under development, and will change more frequently. Simulations with different stimuli are common. Users are unconcerned about VHDL-model-implementation particulars, but may want access to important VHDL model data, such as register values. Like the VHDL designer using Leapfrog's Model Import feature, the Verilog-XL user isn't impacted by a performance penalty for utilizing this co-simulation approach.

In addition to directly linking the simulation kernels, Cadence's approach with Verilog-XL and Leapfrog VHDL is to define an interface or encapsulation layer between unlike language models so that issues like synchronization, signal resolution, and timing concepts can be handled systematically. Due to Verilog and VHDL language differences, slightly different strategies are used for the two types of model import. Engineers can import Verilog models into a Leapfrog VHDL-based design with a VHDL shell created using the Foreign attribute defined in the IEEE 1076/93 standard. Verilog models to be incorporated into a VHDL design will have a corresponding entity-architecture pair declared in VHDL.

VHDL Model Import is slightly different. Because Verilog doesn't have a predefined attribute like VHDL's Foreign attribute, the correspondence between Verilog and VHDL modules is done by convention using an attribute notation. The shell model contains only port definitions. The master simulator (in this case, Verilog-XL) defines the name of the VHDL simulator, and the attribute model specifies the name of the VHDL library, entity, and architecture of the user's VHDL model.

Contributed by Victor Berman, ASIC engineering manager, and Steve Caplow, director of VHDL simulation marketing for the HDL Design Group of Cadence Design Systems Inc., San Jose, Calif.

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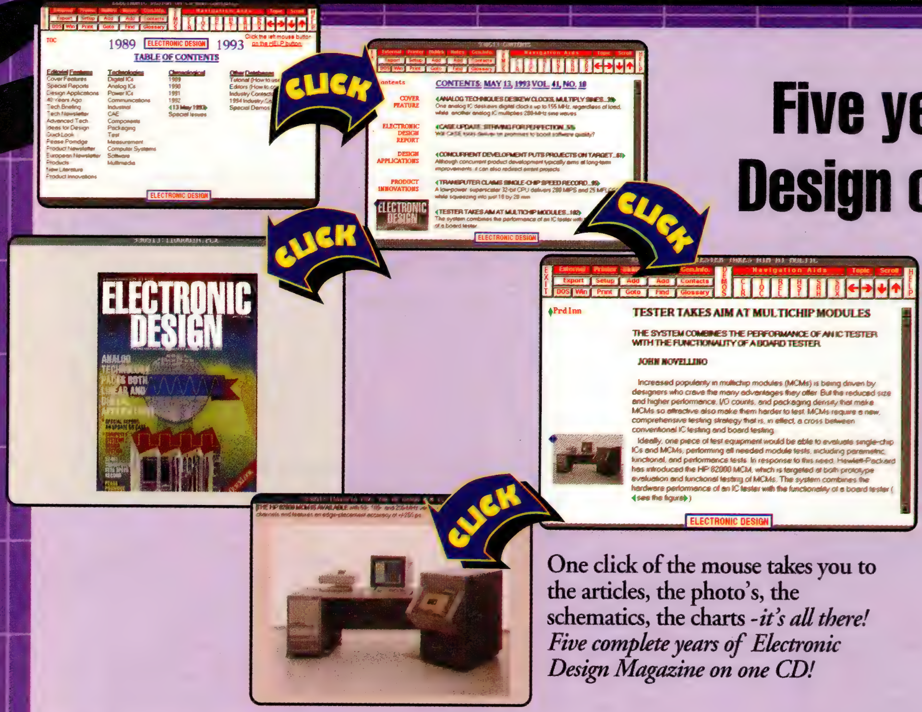

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure)

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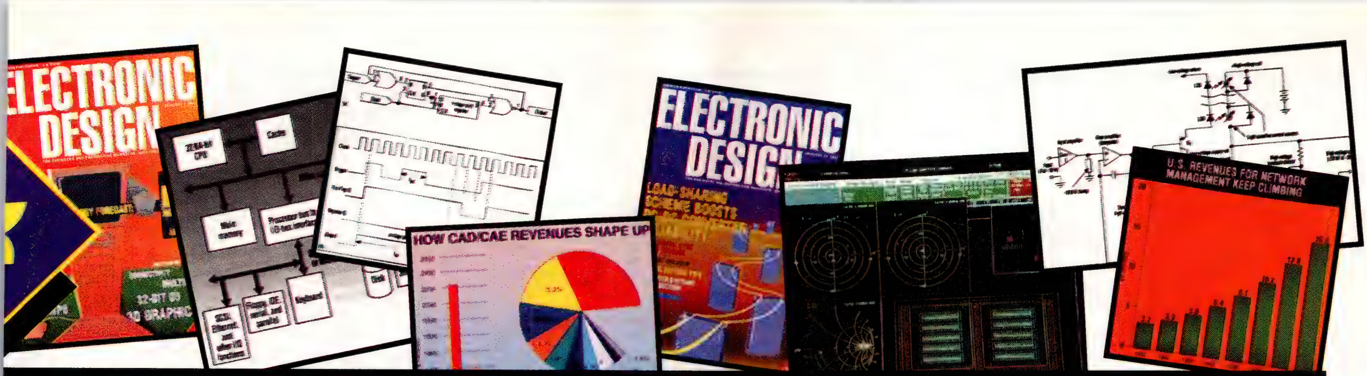
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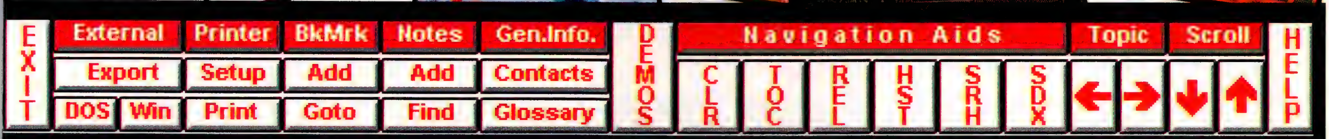

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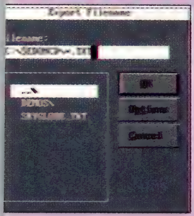

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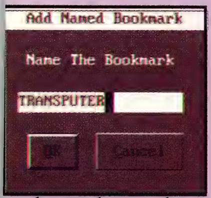

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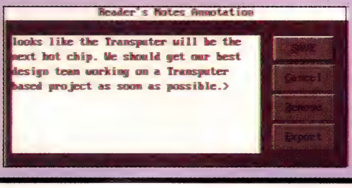

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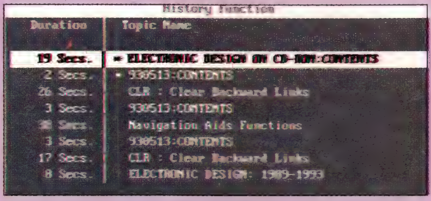

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 Duration   Topic Name

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   2 Secs.  * 930513:CONTENTS
  26 Secs.    CLR : Clear Backward Links
   3 Secs.    930513:CONTENTS
  38 Secs.    Navigation Aids Functions
   3 Secs.    930513:CONTENTS
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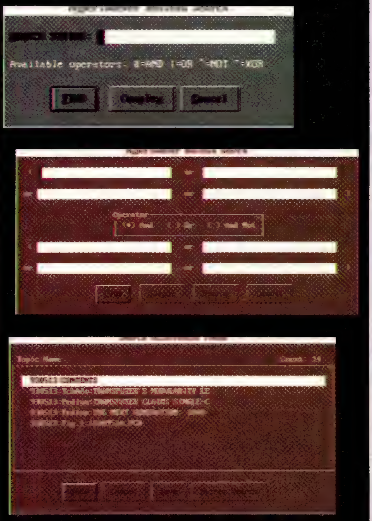

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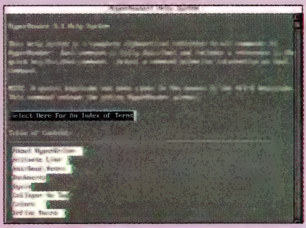

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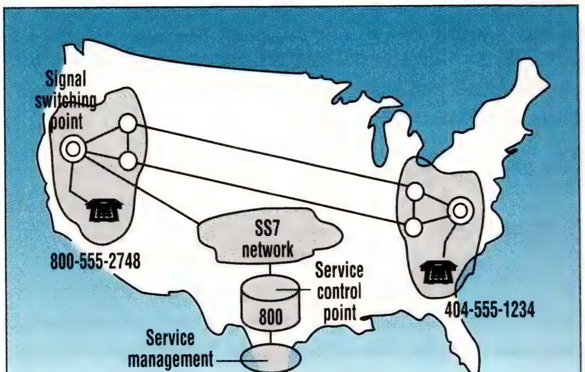
INTELLIGENT NETWORKS: NEW TECHNOLOGY, NEW OPPORTUNITIES

Does The Computer Make The Network Or Does The Network Make The Computer? Find Out As We Explore This Exploding Technology.

BY LEE GOLDBERG

The intelligent network, a marriage of computer and communications technologies, has matured just in time to play a key role in the turbulent communications revolution. While sometimes over-promoted as a universal solution, the concepts behind intelligent networks represent a fundamental shift in the way communication is handled, and will impact most network technologies by the end of the century.

As 1994 draws to a close, most of North America will have access to the "Advanced Intelligent Network," AT&T's version of intelligent-network technology. Designed to add flexibility to the telephone system's infrastructure, the advanced intelligent network lays the foundation for new services, such as mixed voice, video, and data traffic on variable-bandwidth, switched lines, and personal telephone numbers that follow a user through the network. Not limited to telephone systems, the concept of the intelligent network applies to local- and wide-area networks as well as other complex systems.



1 Address translation for 800 numbers is handled by a centralized database within the intelligent network. The signal switching processor within the local exchange recognizes and intercepts the 800-prefixed call and launches a query through the SS7 network. The service control point containing the address-translation table returns the proper routing to the signal switching point, along with billing instructions that send the charges to the receiving party.

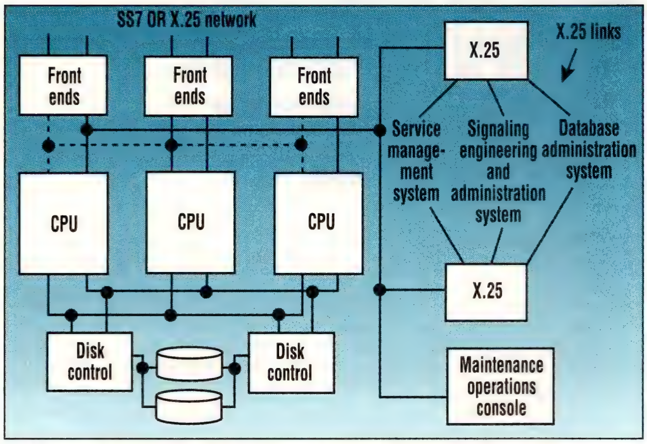
The term "intelligent network" resists a simple definition. What makes it so elusive conceptually is the fact that it's not a single technology. In fact, for the most part, it's really not a new technology but rather the evolutionary by-product of a melding between two technologies, switching and computing technologies.

By taking the root-sum-square of the prevailing industry hype, we can derive a good working definition of the intelligent network: An interconnection system that can implement significant changes to its attributes and functional behavior through software means instead of hardware. In addition, the architecture of intelligent networks is structured to permit centralized modification of system-wide control functions. This ensures that new functions and services can be quickly deployed on the intelligent network and behave exactly the same throughout the network.

But just what does this really mean? Generally speaking, networks will begin to look more and more like computers. If we had to swap out display cards and keyboards every time we stopped using a spreadsheet and wanted to play Tetris, computers wouldn't be terribly useful. These days, the only reason we reconfigure our computer's hardware is to add more capacity or functionality. Until recently, however, this wasn't the case with the telephone system.

NETWORK EVOLUTION

A better perspective on the intelligent network can be constructed by closely examining telephony developments. Held over from its inception in the 1920s, the telephone system's architecture was based around a simple model of renting out sets of wires with a fixed bandwidth to a customer for a given period of time. Much like its contemporary,


SS7 OR X.25 network
Front ends
Front ends
Front ends
CPU
CPU
CPU
Disk control
Disk control
X.25
X.25 links
Service management system
Signaling engineering and administration system
Database administration system
X.25
Maintenance operations console

2. The system architecture of a service control point shows how the redundant CPUs share resources for increased reliability. Connected to the signaling network by either SS7 links or X.25 lines, the service control point's CPUs also are connected to the network's maintenance and control infrastructure.

the Model T Ford, you could have it in any color you wanted, as long as it was black.

Features such as automatic call routing were first implemented with relay logic, following the simple model of telephony developed at the turn of the century. Human operators gave the network some level of intelligence, but its basic structure made providing any sort of non-standard feature, such as three-way calling, call forwarding, or toll-free numbers, a difficult or impossible task.

In the following decades, the technology behind the telephone dramatically improved the reliability of the network, its capacity, and the speed at which it could handle calls, while the model of how telephone service looked to the customer changed very little. Behind the scenes, however, the computer was rapidly replacing fixed relay logic with programmable logic to drive the switching gear, thus providing the foundation for a more flexible infrastructure.

Another important change in the switching architecture occurred when the signals that controlled the routing of calls were moved to a separate channel, known in telephony jargon as "out-of-band signaling." This meant that a second infrastructure grew up in parallel to the voice channels, and it was devoted exclusively to carrying routing and billing information between telephone switching exchanges. Initially, signaling was done using audio tones, but has been replaced in most cases by pure digital transmissions.

The outgrowth of these two technologies is the electronic switching system (ESS), which made its debut in the 1960s. In the past three decades, ESS has reached its seventh (SS7) incarnation and has become a de facto standard for all telephone exchanges within the U.S., Europe, and many other countries.

This new switching technology gave the telephone system the flexibility it needed to provide the user with expanded services. Thanks to the programmable switch, custom routing schemes could be developed for special categories of calls, defined by things like area code, the exchange number (the first three digits), time of day, or the originating party's location.

SS7 IN ACTION

If you dial a toll-free number, your local exchange recognizes the 800 prefix as a special case and doesn't immediately route the call. Instead, it hops on the signaling network and places a query to a large national data base that gives the local exchange two important pieces of information required to place the 800-prefix call *(Fig. 1)*. First, it translates the toll-free telephone number into a standard-format number that can be used to direct the call through the network. Along with address translation, the database provides the billing instructions that direct the toll to be charged to the receiving party.

Similar functions are performed for credit-card, calling-card, and 900-number services. The address-translation capabilities of an intelligent network may eventually provide location-independent personal telephone numbers. This service could enable the network to locate a subscriber and route an incoming call to the user's choice of a personal communication system (PCS) or cellular handset, a nearby wired telephone, or even a network-based voice-mail system.

Because the call routing and billing is handled by programmable computers and not fixed relay logic, it's relatively easy to develop software that provides different combinations of network services for each category of calls defined. This ability to program new responses to service requests is the foundation of intelligent-network technology. The programmable nature of local exchanges makes it possible for the telephone company to offer various services that jack directly into the network's signaling system, such as call waiting, call forwarding, caller ID, and last-number redialing. The uniform network interface that the SS7 signaling protocol provides also enables equipment to be installed in the system, providing new services such as voice messaging, e-mail, text-to-speech services, and database access.

NETWORK ELEMENTS, SYSTEMS

From a broad perspective, the telephone system is divided into two general categories of functions. The *network elements* are the portions of the system that actually carry customer calls and the information required to route them, while *network systems* handle control-related functions such as service control, service applications, billing, and capacity management.

Local exchanges connect a customer's equipment to the network through what is called "the last mile" of wire (or optical fiber cable). In residential applications, the local exchange acts as a network interface for anywhere from 1000 to 100,000

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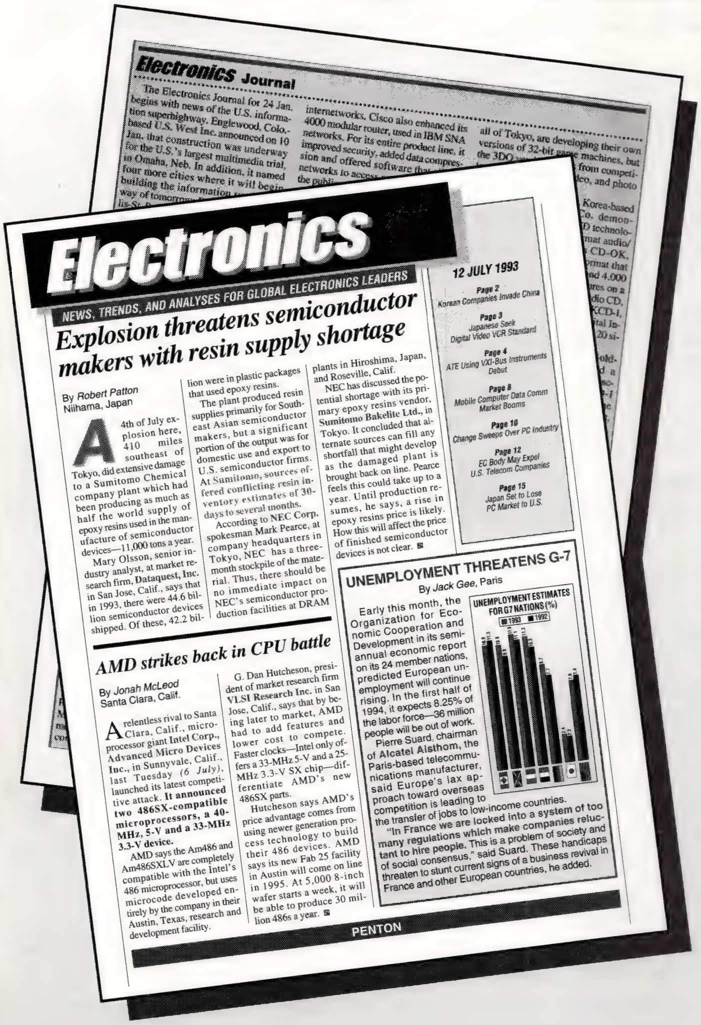

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

internetworks. Cisco also enhanced its 4000 modular router, used in IBM SNA networks. For its entire product line, it improved security, added data compression and offered software that

all of Tokyo, are developing their own versions of 32-bit

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

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Japan Set to Lose PC Market to U.S.

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ■

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ■

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of **Alcatel Alsthom**, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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RESOURCES FOR THE INTELLIGENT NETWORK SYSTEMS DEVELOPER

For those brave souls who are beginning to scout the intelligent-network frontier for opportunities, you will need a few guidebooks to acquaint yourselves with the territory. Here's a short collection of materials you may find useful:

The Bellcore Information Center: Why not get your information straight from the source? The Bellcore Information Center has a very extensive technical library open to the public, with reprints available for sale. In order to navigate this vast collection of information, you'll need *The Bellcore Library Catalog.* Because the library is so vast, they offer a catalog in both printed and electronic form. To obtain a hardcopy catalog, just call the center at (800) 521-2673 or (908) 699-5800. Better yet, you may reach the on-line catalog either over the Internet or via conventional dial-up services. For the Internet, it's: telenet—info.bellcore.com; At login prompt, respond with: CAP10. For dial-up, it's: (201) 829-2005 - at annex prompt; respond with: Telenet—info; At login prompt, respond with: CAP10.

The electronic catalog is updated weekly and may be searched by subject, author or title. Each entry contains an abstract, document reference number and price. An invaluable (and free!) reference tool.

While the Information Center can supply you with documents on nearly any aspect of communication and telephony, there are two publications that you can't afford to be without:

- *The Advanced Intelligent Network* - Document number SR-NWT-002247. This document was written to provide a high-level view of the level-1 architecture of the advanced intelligent network as it exists today. If you need a good primer on advanced-intelligent-network technology and the Bell System technical culture, this is it. Price: $92.00.
- *Network Equipment Building Systems (NEBS) - Generic Equipment Requirements* - Document number TR-NWT-000063. If you're going to try to sell equipment to a North American telephone company, this is your bible! Learn from the folks who defined reliability. Covers everything from switching components to wiring and installation practices. This is the telecommunication world's version of the MIL-SPEC. Price: $80.00.

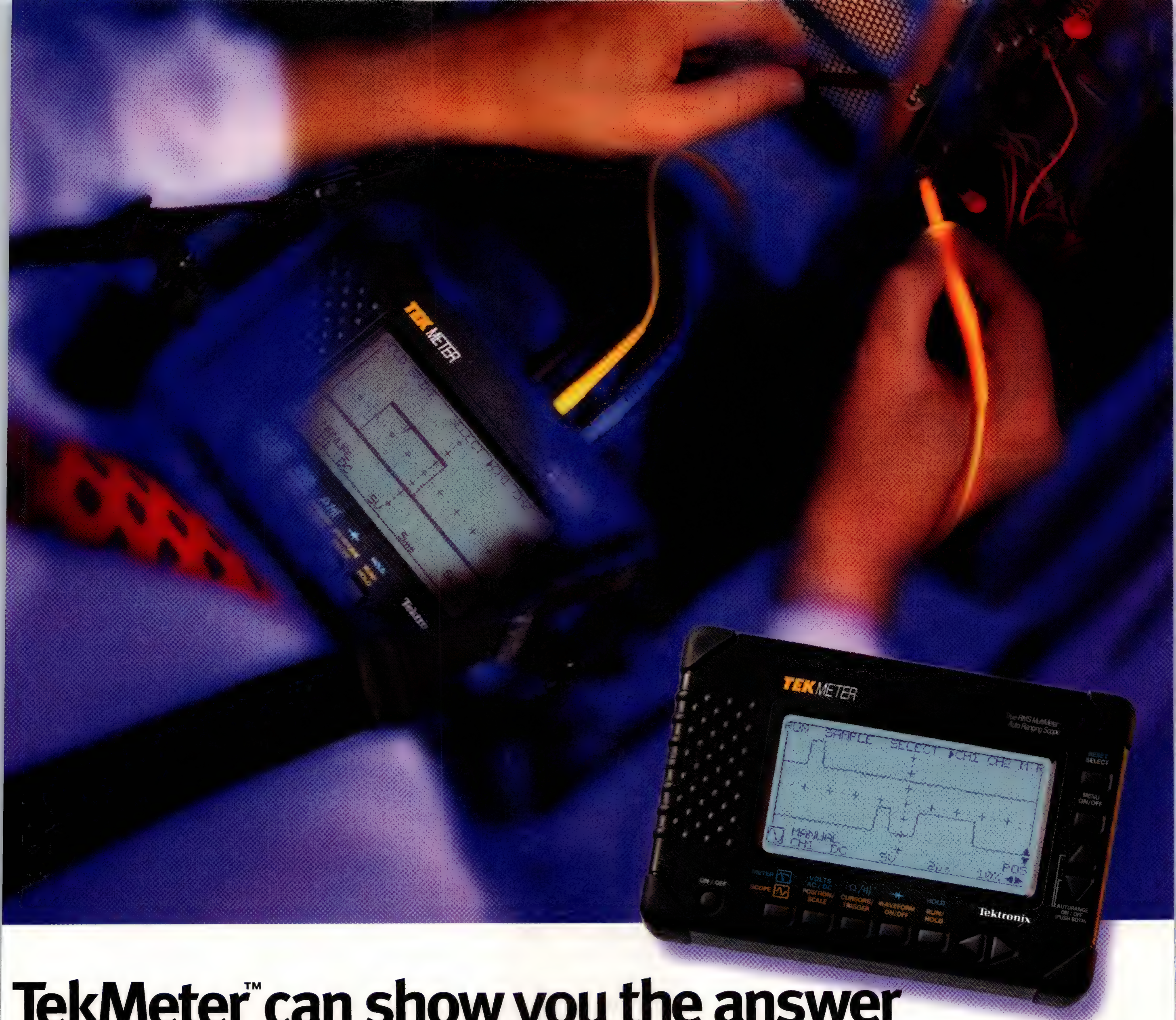
Contact the Bellcore document order line at (800) 521-2673 for these and all other Bellcore documents.

Another great source of information is **The IEEE Library**. Over the years, the IEEE Proceedings along with its companion publications *Networks* and *Communications* have covered intelligent networks extensively. The IEEE library also has conference proceedings and papers on file. Members can call the library at (908) 562-3794 and request a keyword search of their catalog. Once you have identified an article you need, a pay-by-the-page reprint service is available for both members and non-members. You may contact them at: ASK*IEEE - ATTN: Manager Document Delivery, P.O. Box 4327, Burlingame, CA 94011; (800) 949-IEEE; fax: (415) 259-5045; internet: askieee@ieee.org. One top-notch paper on intelligent networks is *The Intelligent Network—Changing The Face Of Telecommunications* by Richard B. Robrock II. This paper gives you a nice overview of the telephone company's vision for intelligent networks. The bibliography alone is worth the price of the reprint. The article appeared in IEEE Proceedings, Vol. 79, in January 1992. IEEE Catalog Number: 9041044.

Other interesting papers include *"New Service Ideas and Intelligent Network Technologies"* by J. Mizusawa and M. Akiyama, *"Intelligent Digital Mobile Communications Network Architecture for Guaranteeing Personal and Terminal Mobility"* by Y. Maruyama, A. Nakajima, and H. Sawada, *"Communication Session Management for Distributed Multimedia Specifications"* by H.E. Bussey and S.B. Weinstein, and *"Future Standardization Issues of Intelligent Networks"* by K. Nagaraj and S. Harris. All four papers were delivered at the "1992 International Zurich Seminar on Digital Communications. Intelligent Networks and their Applications", Mar. 16-19, Zurich, Switzerland. They're available in the conference's proceedings (IEEE Catalog Number 92TH0439-0).

If you're still hungry for additional information, you might consider looking at these:

- *SS7 Basics*: by Toni Beninger. This pithy book will familiarize you with some of the intricacies of the SS7 signaling protocol. A very helpful primer and basic reference tool. Price: $29.95. Contact: Telephony, P.O. Box 12901, Overland Park, KS 66282-2901.
- *"The Death Of Telephony"*: By George Gilder. Published in the Sept. 11 edition of *The Economist.* This little piece gives some thought-provoking perspectives on intelligent networks and the future of the telephone system. Gilder's claim is that a central telephone system with fixed-bandwidth voice channels is going the way of the vacuum tube and buggy whip. Even if you don't agree, he makes some powerful points and questions some of the most basic assumptions we have made about communication technology. Gilder also is a regular contributor to *ASAP,* the quarterly technology supplement to *Forbes Magazine,* where he engages in a lively discourse on various communications-related subjects.
- *"Strategies and Solutions for an Open Telecom World"*, available from Chorus Systems, 15262 NW Greenbriar Pkwy., Beaverton, OR 97006.



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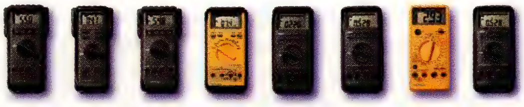

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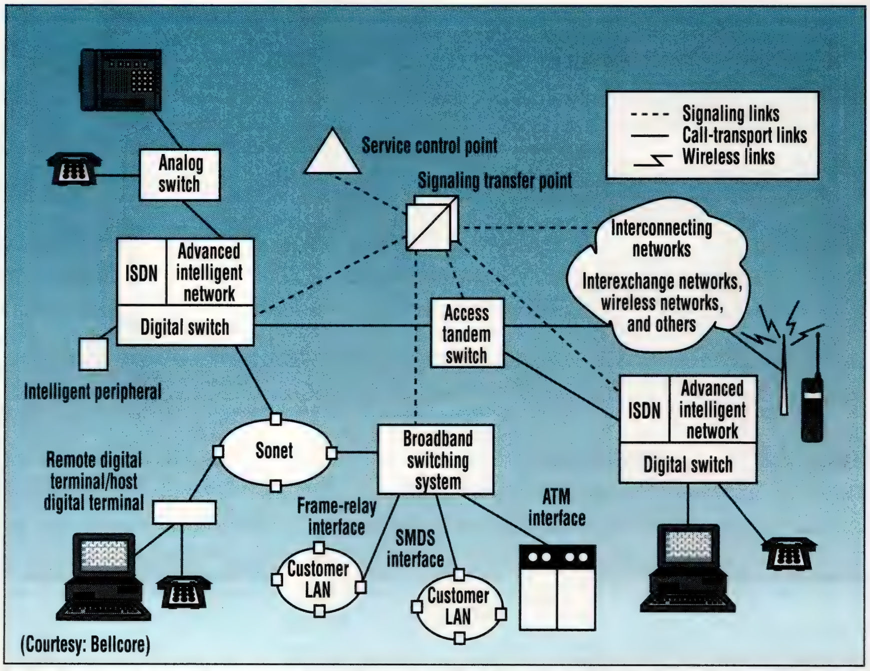
telephone lines and provides local call switching. A local exchange is a collection of one or more units called signal switching points that have been bundled together.

Signal switching points (SSPs), one of the most common network elements, are located within local exchanges and serve as the interface between customers and the rest of the intelligent network. The signal switching point is a stored-program switch that takes customer calls and generates routing signals which are sent into the SS7 signaling network via 56-kbit/s links. While these switching elements are relatively "dumb," they're programmed to recognize and intercept calls that require special handling, as well as launch queries to centralized data bases for the purposes of call routing and billing instructions.



(Courtesy: Bellcore)

3. The intelligent network can act as an on-demand wide-area network to bridge local-area networks, cellular systems, and other networks. Using the intelligent network's capabilities, a business can extend the office local-area-network environment to remote locations, home offices, and mobile workers. The switched connections permit on-demand service, which is ideal for applications with insufficient traffic to justify a dedicated line.

Signal transfer points (STPs) usually lie deeper within the network, functioning as high-capacity, high-reliability packet switches that carry signaling information between the message-carrying side (network element) of the network and the signaling and control (network system) infrastructure. The signal transfer point's basic function is to route the signals from one switch to another, or to and from the large databases within the network control system.

Signal inputs to the signal transfer point usually consist of between 256 and 1024 56-kbit/s SS7 network connections. Under normal operating conditions, a signal transfer point will process between 1000 and 5000 signaling packets per second.

Since they're connected to many switching nodes and cover large service areas, signal transfer points are run in fully redundant pairs that are geographically separated to guard against a natural disaster affecting both units. A single signal transfer point can handle the total regional traffic load. But under normal circumstances, the pair distributes the load between themselves to guarantee that either unit is fully functional in case of a possible disaster.

THE BRAINS

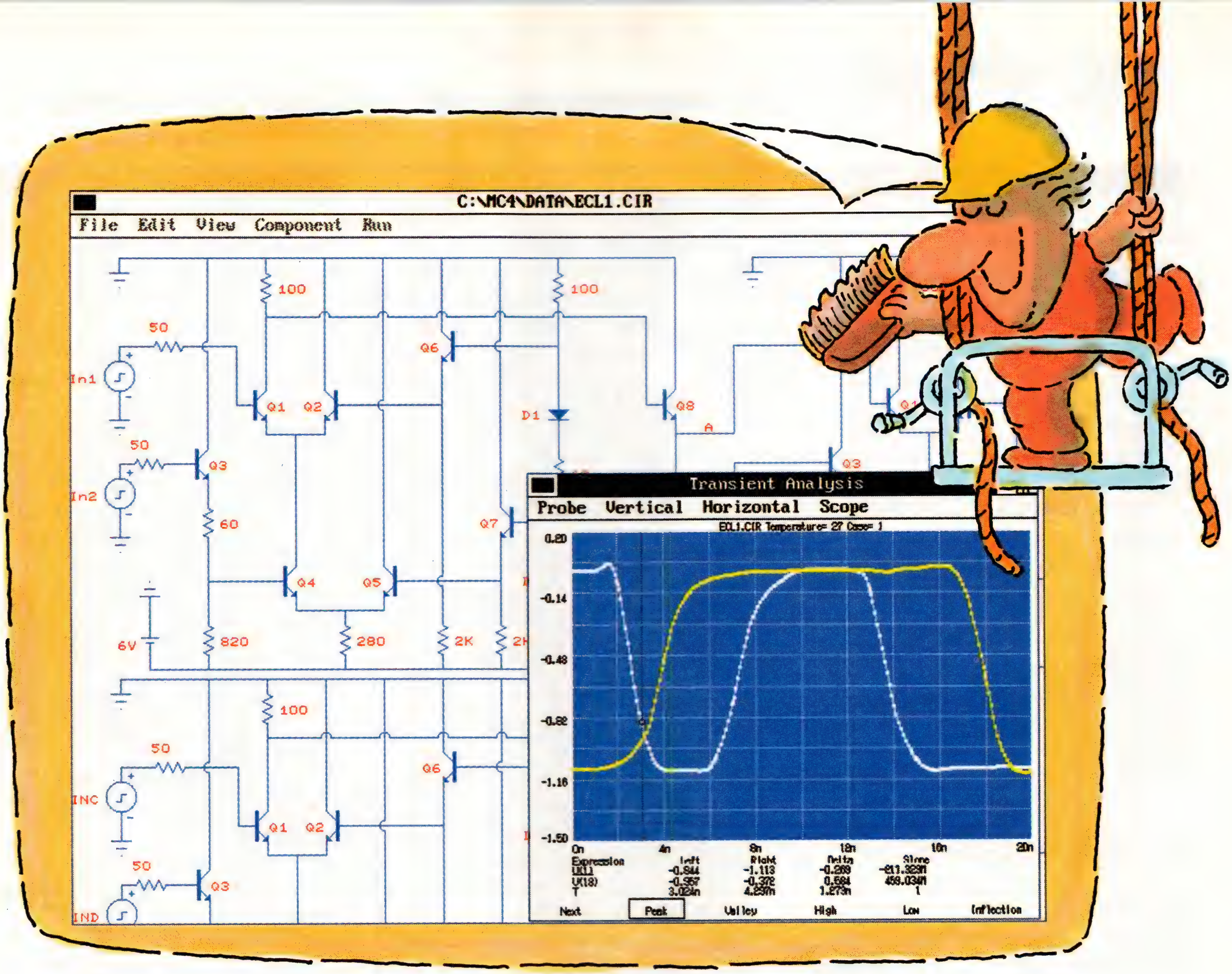
The service control point (SCP) is a highly reliable, on-line data base that gives the intelligent network its "brains." This unit supplies the switching system with customized information on how to deliver and charge for special services or features requested by a specific user.

Service control points provide call-handling information to the network's switches and service transfer points at rates of up to 300 calls per second. These units support regional and national services, such as routing and billing information for 800- and 900-number services. Alternate billing (credit card/calling card) services and special business services (e.g., virtual networks) also rely on service-control-point databases.

Based upon a multi-CPU architecture, the service control point is interfaced to the network via multiple SS7 or X.25 communication links *(Fig. 2)*. All CPUs share a common disk farm and a common interface to the signaling engineering and administration system that monitors and controls the network's configuration.

To ensure that the service-control-point's database is always properly configured, it's tied to a database administration system and a service-management system. Another link to a maintenance operations console (MOC) provides network administrators with an ongoing appraisal of the service-control-point's health status.

An adjunct is a junior version of the service control point. Designed for work within a telepone local exchange, the adjunct supports call setup and local intelligent-network functions known as custom local-area signaling services (CLASS). CLASS includes call such services as waiting, last-caller ring-back, call forwarding, and caller ID. Signaling between the adjunct and its local signal switching point is done through the Ethernet, while SS7 links are used to communicate with service control



Expression	Left	Right	Delta	Slope
V(1)	-0.844	-1.113	-0.269	-211.329M
V(18)	-0.957	-0.372	0.584	458.034M
T	3.024n	4.297n	1.273n	1

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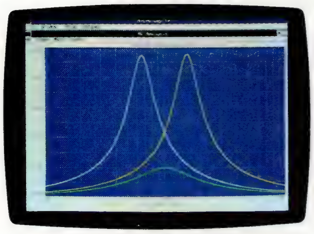
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INTELLIGENCE—A MATTER OF LOCATION

It seems as though its difficult for any two communications systems designers to agree on a definition of intelligent communications. However, they may be just disagreeing on where the intelligence should be, or which part of the total system should be the "dumb" portion.

One easy way to compare different interpretations of "intelligence" is to spell out the two prevailing definitions. The "centralized intelligence" view, adopted by most of the telephone companies and many of their suppliers, includes the diehard PBX "mainframe" suppliers and some of the wide-area-network multiplexer suppliers. The alternative is the "peripheral intelligence" perspective, embraced by many telecommunications equipment manufacturers and the computer telephony community (which includes companies that incorporate telephony expertise in the computer chassis). This view downplays the idea of central switching control, instead favoring the idea that bandwidth should be extended at the desktop level and along the "edges" of the system. This is where users can best define their applications using new microelectronics and software capabilities.

There are obvious conflicts. In the traditional telephony world—as envisioned by the telecommunications and regional Bell operating companies—small amounts of bandwidth are metered out to customers from intelligent central switches. In the wide-area network, the telephone companies compensate for narrow-band channels with complex electronics, using advanced compression technology like ADSL to cram compressed video images into already-installed twisted pairs.

The "central intelligence" view may certainly relieve the network from dealing with large torrents of data by making the central switches increasingly smart, providing all kinds of services from caller ID to intelligent voice/facsimile services. This "central intelligence" ignores the inherently large-bandwidth carrying capacity of installed fiber in the network. In fact, it actually has led to denial of leases on "dark fiber" (fiber not limited by telephone-company protocols), as well as the requirement that only the telephone companies provide services. For on-premise environments, new ICs and software are available that build on the fundamental idea of dumb isochronous networks. While electronic bottlenecks potentially reduce the performance of these ICs, they can be interfaced to standard Sonet framers that provide plenty of on-premise bandwidth for existing and future applications. What results is a potential range of "dumb distributed networks" which can be constructed inexpensively and use 51- or 155-Mbit/s Sonet links to connect multimedia servers for all types of traffic. Isochronous distributed switching is a key attribute of the new ICs, enabling even advanced asynchronous-transfer-mode (ATM) networks at the periphery.

Many leading suppliers and carriers, ranging from IBM to MCI and including Mitel, now embrace this "periphery" view, and are trying to move as much flexibility as possible to the users' location at the desktop. The IC capabilities and software tools are the focus of the companies' efforts. The key is bandwidth, an ideal substitute for central switching, which makes possible "virtual" switches that permit each terminal client to listen to messages on individual wide data pipes, characterized by low latency and high bandwidth.

To achieve these high-bandwidth, low-intelligence connections, they're providing special computer telephony ICs and associated software systems to communicate from the host computer to a distributed central switch through open communications protocols. Tools are available to provide a switch-to-host link that's mapped to specifications through a PBX driver. External applications can be connected easily to open, dumb PBXs. The technology can supply expanded user networks that distribute more data to dispersed sites, with 3D graphics and other visualization tools.Even MIS managers at large companies, typically known for an affinity for central control, indicate that a flexible, inexpensive connection to a "dumb" bandwidth is desirable between dispersed resources.

In the small business office, or the home, bandwidth can be easily expanded by using existing cable lines as a bandwidth pipe. Couple the cable pipe with the appropriate shrink-wrapped application and a cable interface card—available from a local computer store—and the home or small office can come "on line" as part of the peripheral intelligence.

Over the long term, an all-optical dumb network can be defined that will have no real bandwidth bottlenecks. Dumb, high-bandwidth fiber connectivity provides an unlimited capability, unrestricted by the limitations inherent in electronic switching. As intelligence becomes more distributed through smarter terminals, the demand for "intelligence" in the network itself will ebb.

The choices, then, lie not in how to define intelligent networks, but where the intelligence is located. At the periphery, it's far more flexible and versatile for the system's users. The alternative is the intelligent centralized communications network driven by large, regional suppliers. Such a network would be based on long-term system restructuring that will take many more years to roll into place than most users want to wait. In effect, it will be smarter to be dumb!

Contributed by Mel Roberts, product manager, Real-Time Networks, Mitel Semiconductor Corp., Ontario, Canada.

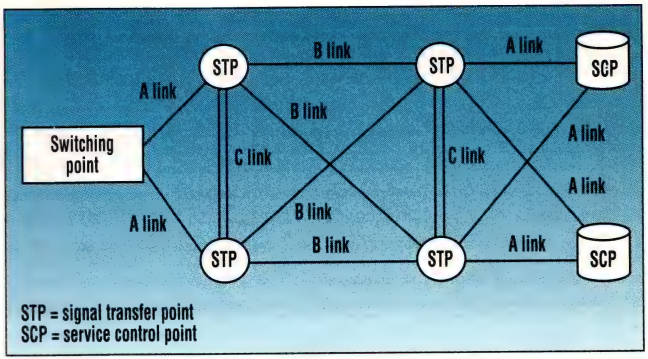
points throughout the network.

Overseeing each regional network is a signal engineering and administration system (SEAS). Linked directly to all of the signal control and transfer points, the SEAS keeps track of the status of every SS7 link under its jurisdiction. It also maintains the routing information used by signal transfer points .

THE VERSATILE PERIPHERAL

One somewhat unique brand of network systems devices are intelligent peripherals, because they can be located either within the network as embedded service providers or attached to the edge of the network by third-party operators who wish to sell their services to network subscribers. Connections to the network are handled much like other intelligent-network boxes, with SS7 links being used for signaling and T1/E1 links for voice/data. The links between co-located intelligent peripherals will be run via Ethernet or some high-speed derivative. For their customer interface, intelligent peripherals can use either conventional analog connections or ISDN lines. ISDN is an all-digital telephone service that supports high-speed data and allows subscribers a limited form of out-of-band signaling (via the "D" channel). Using ISDN, a subscriber can send and receive control information from the intelligent peripheral and perform call setup to access other network functions.

The current generation of intelligent peripherals are being used to perform tasks similar to adjuncts such as voice messaging, voice response, and voice recognition. If telephone companies have their way, the next generation of advanced intelligent peripherals will be able to offer more sophisticated services, such as video-on-demand and direct access to the Internet.



5. The redundant interface between STPs and SCPs provides highly reliable service that can't be interrupted by the failure of any single link or element. Different links to the SCP are defined for access, bridging, and cross-linking (A, B, and C, respectively).

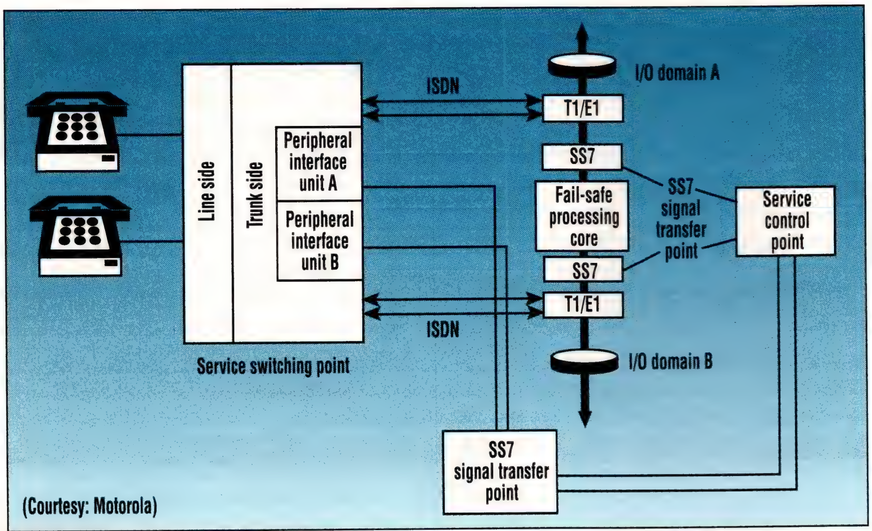
The architecture of the intelligent network also has been designed to facilitate the integration of local-area networks, cellular radio systems, and other types of networks *(Fig. 3)*. This would allow customers to treat the telephone system like an extension of their own local network by providing on-demand, switched, wide-area-network (WAN) services. The on-demand WAN will offer a great value to the many businesses with operations in several locations but insufficient traffic and/or capital to justify a dedicated link to each site.

WHERE'S THE INTELLIGENCE?

To understand why today's intelligent network looks so different from most networks, one must understand the history behind the telephone system. The current telephone system grew out of a control structure that was developed to tie together an enormous network using the simple technology available at the time. Due to the size of the network, automation didn't come in a single step, but rather in small increments over a period of four decades.

Human operators were phased out of local and then long-distance calling as the telephone system was slowly automated by system engineers. These engineers used relay logic to implement complex tasks—like random-access call switching and billing based on distance and connection time.

The tightly held control system mimicked the hierarchical command structure used by the human operators. This was deemed necessary to maintain order within the vast telephone-network empire, to ensure that network services worked the same throughout


Line side
Trunk side
Peripheral interface unit A
Peripheral interface unit B
Service switching point
ISDN
ISDN
T1/E1
SS7
Fail-safe processing core
SS7
T1/E1
I/O domain A
I/O domain B
SS7 signal transfer point
Service control point
SS7 signal transfer point

(Courtesy: Motorola)

4. The block diagram of an intelligent peripheral illustrates the modular nature of intelligent-network system components. Designed to provide services like voice response and recognition, special-toll services, and voice messaging, the intelligent peripheral consists of redundant processors linked to a service control point via the SS7 network. Interfaces to message traffic are done through standard T1/E1 connections to the trunk service. Most components within the intelligent peripheral are available as standard OEM modules and may be used in other network elements such as service control points and adjuncts.

the country, and so that the system's resources were used efficiently.

When expensive mainframe computers were introduced in the 1960s, it made sense to maintain the paradigm of centralization to reduce the number of databases that had to be managed, and to most efficiently use the high-cost facilities. Today's system still reflects many of the structural decisions that were made during this time. As an example, the routing for all 800-prefix telephone calls is still handled by a single database system that's located in Kansas City, MissouriB(B+B.B1DB5^{5}P̈volutionary approach improved performance while preserving the network's integrity. What was sacrificed along the way was some of the potential flexibility offered by programmable switching technology. Despite all of the new computer systems, adding new services or features to the large, centralized infrastructure always involved millions of dollars in capital and years of time.

The intelligent-network strategy developed by AT&T is an attempt to reengineer their telecommunications network into a more flexible system while still retaining a fairly centralized control structure. As microcomputers have become less expensive, more plentiful, and readily available, network intelligence has seen an outward migration to regional and local areas, but the control has remained concentrated in one point.

In contrast, some equipment manufacturers have taken advantage of this inexpensive computing power and put it to work at the network periphery in the form of the private branch exchange (PBX). Originally developed for business applications, the PBX places intelligence and control at the network's edge. Besides providing an interface between an office's telephones and the outside world, the PBX can provide sophisticated services such as voice-mail, call forwarding, selective screening of incoming or outgoing calls, and selection of long-distance carrier based on lowest cost for a given time of day and destination.

Some advocates of PBX technology say that this decentralized approach may be more cost-effective and efficient for larger applications, too. For instance, in developing countries like China or Brazil, PBXs sometimes are used as local exchanges for villages and outlying areas, tying an area's telephones together with a smart switching system and providing long-distance service through a limited number of tie-lines to the country's national infrastructure.

While the intelligent network works well, it may be a triumph of engineering over common sense. Some prominent critics argue that a network with distributed intelligence and control is more efficient, easier to upgrade, and less expensive than a centralized-control one, especially in terms of bandwidth-minutes-per-dollar *(see "Intelligence: a matter of location," p. 80).*

As previously mentioned, most of North America will have access to AT&T's Advanced Intelligent Network, which is the company's version of intelligent network technology. Around mid-1995, AT&T plans to open up the network to other service providers, according to Dave Maruitak, a senior member of the technical staff at AT&T Network Systems, San Diego, Calif. He sees this as a great opportunity for persons interested in providing niche services for specific geographic regions, specialized business or professional communities, or other targeted market groups.

NETWORK ENTREPRENEURSHIP

Once the telephone network adopts an open architecture, the intelligent peripheral will be a key tool for entrepreneurs who wish to sell services over the telephone system. Because intelligent peripherals behave as true peripherals to the network, they can be employed either as gateways to other networks or as large, remote disk farms for centralized archiving and database management. Located at the periphery of the network, these privately owned intelligent peripherals will be able to offer their clients backup services for distributed networks, on-line databases, specialized switching networks, foreign-language voice-recognition/response services, and even accelerate the onslaught of interactive home-shopping clubs.

Besides providing programming and information services, many other business opportunities are opening up within the intelligent-network world. For those wishing to develop intelligent peripherals or other telecommunication products, the highly defined open-system environment of modern telephone systems gives potential vendors a running start.

The evolution towards an open-systems architecture is a beneficial by-product of the move toward a standardized national intelligent-network infrastructure. As the telephone-network architecture developed, it became increasingly dominated by computer technology. By 1980, when the SS7 switching system began development, the decision was made to use an open-systems approach and a layered protocol much like the open systems interconnection (OSI) reference model successfully employed by the International Standards Organization (ISO) in the data-processing world. In compliance with the open-systems approach, software for network products now is written almost exclusively for a Unix environment, most often in the C or C++ languages. This new paradigm reflects today's trend towards the client-server model for data networks. In this case, the customer is the client and the service control point is the server, providing connections to intelligent peripherals and adjuncts throughout the network.

Most modern telephone equipment is built from different combinations of the same basic components. The open-telephony-platform model, for instance, has encouraged a building-block strategy

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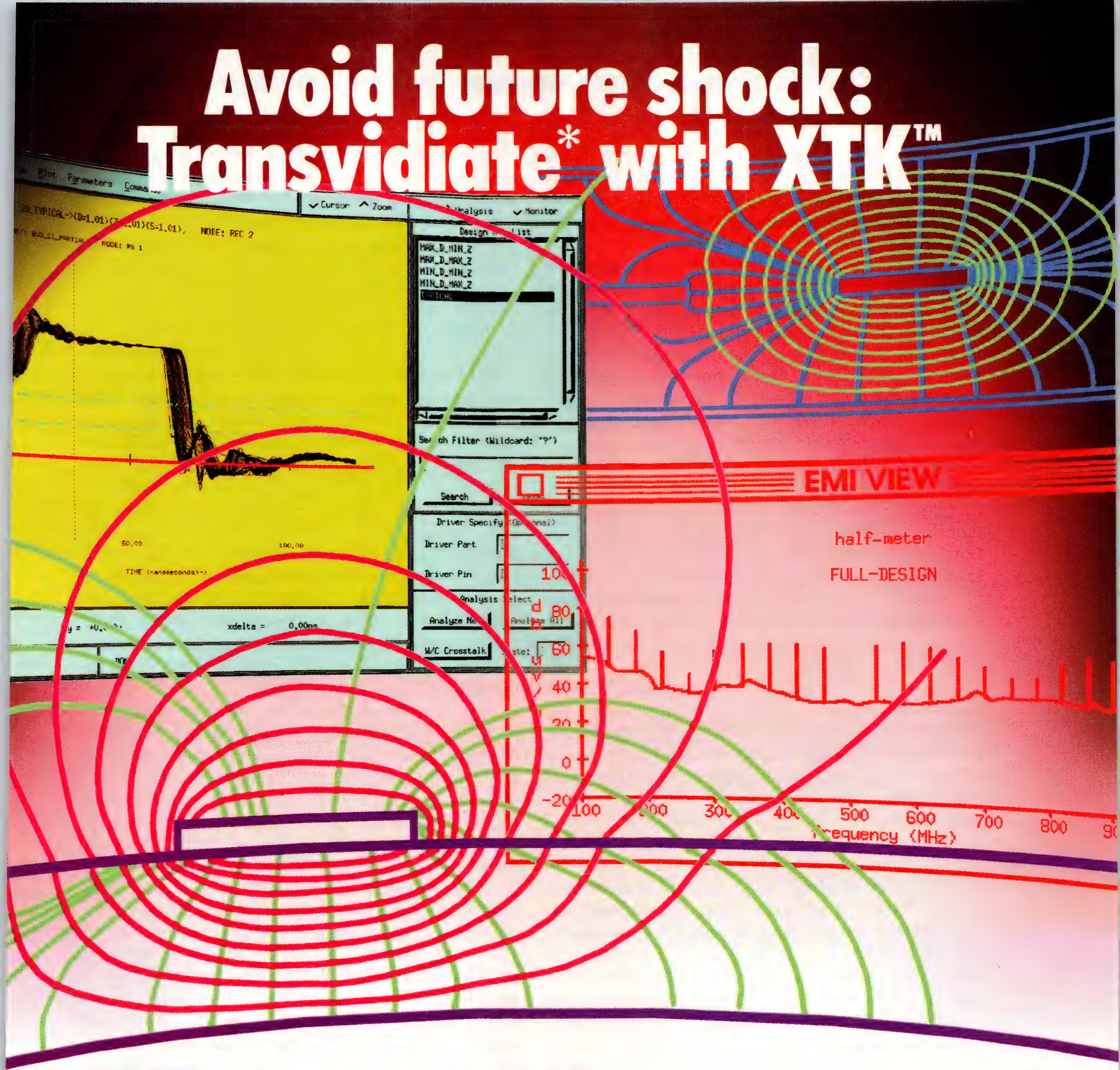

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for network development, where specialized components are constructed from generic computer equipment and telephony interface hardware and then is customized using Unix-based, application-specific software *(Fig. 4)*.

At the center of nearly any network element or system is a computer with a redundant architecture, which usually sports a large disk array to house the databases associated with its applications. One or more 56-kbit/s communication ports are used for SS7 signaling to the network, while an Ethernet or other high-speed local-area network often is employed for data transfers between devices within the same facility.

A word of caution is in order, though, for those enterprising souls who are already dreaming of reaping the treasures of the intelligent-network frontier. Despite many similarities to the conventional data-processing world, it should be noted that network and data-processing types will probably suffer serious culture shock upon their first exposure to the insular world of telephony, which has had a hundred years to develop its own approach to everything.

Not only is there lots of new terminology, buzzwords, and jargon to assimilate, but also a very different way of looking at networks. As an example, many network block diagrams used by the phone system devote only passing attention to the actual voice carrier channels and tend to concentrate almost exclusively on the much more complicated signaling infrastructure. One key to understanding how telephone systems are assembled is to remember that reliability is almost a religious issue in the telecommunications world. For regional services such as service control points, the maximum allowable down time is measured in minutes per year. To achieve this, any important system element must be supplied as a redundant pair, with any single unit capable of doing the job. The cross-strapping arrangement illustrated for a typical connection between a signal transfer point and a service control point is a good example of the redundant architecture used throughout the system *(Fig. 5)*.

STRICT REQUIREMENTS

In addition to redundancy requirements, all equipment used within the telephone system must conform to stringent mechanical and electrical requirements set forth by Bellcore in its Network Equipment—Building System (NEBS) generic equipment requirements standards. These specifications dictate the mechanical and electrical performance for each type of component. Among other things, a NEBS-compliant computer must be able to run on 28-V dc standard telephone-company power; support the Unix operating system; pass rigid flammability tests; be able to operate continuously in a dusty, non-air-conditioned environment; and survive a zone-4 earthquake.

One approach to meeting these stringent requirements is to purchase OEM equipment from telecommunication-smart manufacturers and provide added-value engineering through system integration and software development. Several companies offer fault-tolerant, network-compatible computer systems that can be mounted directly into a standard-size telephone-equipment rack. Vendors of NEBS-compliant equipment include IBM, Motorola, Stratus Computer, and Tandem Computer.

For low-volume applications or operations where development capital is limited, purchasing OEM modules and software can dramatically reduce up-front engineering costs. As an example, The Motorola Computer Group offers a complete line of open-network system platforms, including the SeriesFT, VMEbus-based computers that feature a fault-tolerant architecture, automatic fault recovery, and intelligent configuration management. The Unix-based software available for Series FT products provides a solid foundation for applications development with a process scheduler, several databases, and code modules which support communications protocols for TCP/IP, X.25, and SS7 signaling networks.

Software development for intelligent-network products also is getting easier as the standards for open-platform telephony become more well defined. One of the most active players in the telecommunications software market is Chorus Systems, Beaverton, Ore. The company's microkernel-based, object-oriented software platform is designed specifically to develop operating systems used in communication products. The Chorus architecture is fully scalable, permitting the same kernel that was originally developed for a PBX or service control point to be used in smaller applications, such as handheld PCS units and small intelligent peripherals, while maintaining the same attributes and protocols. The code's modular design also makes maintenance and upgrades easier and quicker to implement. Though originally developed for telephony, Chorus also has been successful in developing data-communication products for local- and wide-area networks.

In summary, the intelligent network isn't a single technology or architecture. Instead, it's an approach to network architecture that permits rapid reconfiguration to support the changing needs of its users. Although nobody can predict what the next generation of networks will look like, you can probably expect that they will borrow heavily on the lessons learned from *today's* intelligent networks.☐

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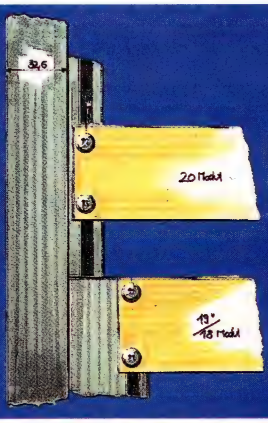

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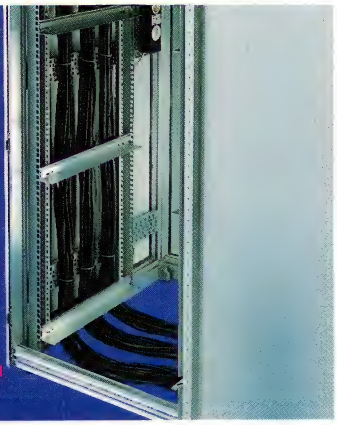

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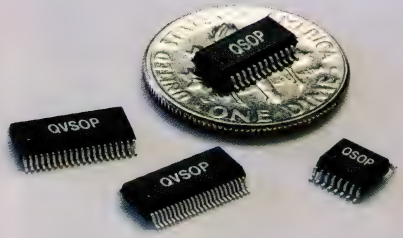

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INCREASE FAULT COVERAGE WITH I_{DDQ} TESTING

As A Supplement To Conventional Tests, Measurement Of Quiescent Power-Supply Current Can Improve Device Quality.

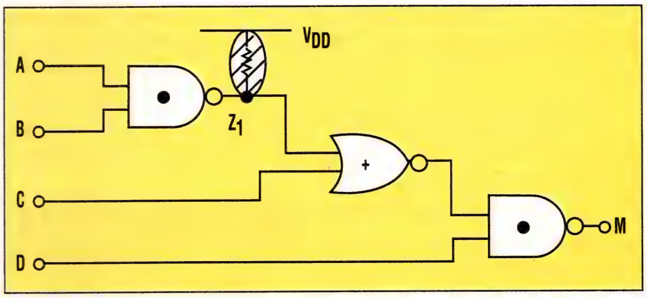
VIC KULKARNI
CrossCheck Technology Inc.,
2833 Junction Ave., Suite 100, San Jose, CA
95134; (408) 435-9100, ext. 206.

Although the adoption of design-for-test (DFT) techniques has risen in recent years, more than 75% of new IC designs don't use on-chip DFT structures. This compromise of testability and quality requirements is done against the backdrop of heavy time-to-market and power/performance pressures. As far as manufacturing test is concerned, only functional logic-level testing is performed, along with dc parametric tests of the IC. But because simulation of vectors is time-consuming and CPU resource-intensive, this important step often is skipped, resulting in low fault coverage for a given set of functional vectors. Consequently, designers may find that I_{DDQ} (quiescent power-supply current) testing is an easy, yet effective, way to increase fault coverage.

In fact, there's been a movement toward measuring I_{DDQ} as a way to supplement conventional stuck-at-fault testing or as a standalone test technique. Many researchers endorse I_{DDQ} testing and have published papers on its merits. Data from leading IC suppliers as well as end users has shown that combining I_{DDQ} testing and functional logic-level testing can boost failure detection by 2% to 11%. One end-user, Storage Technology, also reports a substantial reduction of early-life system failures when using I_{DDQ} testing as a screening technique for incoming inspection at the IC level.

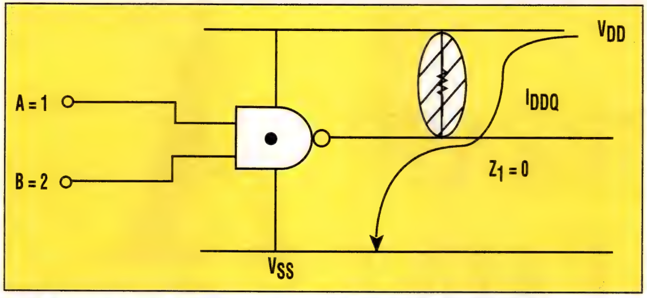
Basically, I_{DDQ} testing offers a way to enhance the quality of IC tests by monitoring the device's power-supply current. The technique applies primarily to digital CMOS circuits, where I_{DDQ} in a defective device can be orders of magnitude higher than in a defect-free circuit. By monitoring the power supply, therefore, designers can detect defects and raise device quality.

Two forms of I_{DDQ} testing are available today. DFT I_{DDQ} testing requires a specific set of test vectors that are obtained from automatic-test-program-generation software. Non-DFT I_{DDQ} testing requires only functional vectors and isn't limited to synchronous designs or to the use of stuck-at models. Instead, non-DFT I_{DDQ} testing uses a minimum set of functional test vectors derived by conventional means, such as functional verification and simulation.



1. IN CONVENTIONAL STUCK-AT testing, four bits are needed to detect the short. Two (at A and B) activate the defect, while the other two (at C and D) propagate the defective behavior to the primary output.

Used alone, non-DFT I_{DDQ} testing is ideal for designs without DFT structures, like scan cells or embedded-grid technology. Typical applications include high-volume, low-silicon-cost situations where silicon area is a premium.



2. IN I_{DDQ} TESTING, FEWER VECTORS are needed because the defective behavior doesn't have to be propagated to the primary output. Instead, the defect causes a measurable quiescent current to flow.

IC manufacturing involves many critical steps, such as metal depositions only a few thousand angstroms thick, submicron photolithography, and etched contact holes a few tenths of a micrometer wide. Small imperfections during these steps can cause randomly distributed defects in the IC, including shorts between metal lines or opens between input signal and polysilicon gate control contacts. Such defects reduce the typical yield in an IC manufacturing process to about 70%.

CREATING TEST PATTERNS

Obviously, testing is needed to identify and eliminate defective ICs or defects within the ICs. In a typical example, a test pattern of A = 1, B = 1, C = 0, D = 1 is needed to detect a short between output Z_1 and the power supply *(Fig. 1)*. The first two bits (A = 1, B = 1) activate the defect so that a faulty behavior is produced. In this example, the test pattern should produce a 0 at Z_1. However, a short between Z_1 and the power supply (V_{DD}) will force the output value to be 1. The 1 in place of the expected 0 identifies a defect.

The remainder of the test pattern (C = 0, D = 1) is needed to propagate the defective behavior to the primary output, M, where a tester can observe the signal and compare it to a good value. For a sequential circuit, the designer must create a sequence of test patterns to sensitize and propagate the defect.

To ensure that no defect escapes detection, this process must be repeated for each possible defective site. The percentage of potential defects found by a test program is known as its fault coverage. The higher the fault coverage, the higher the quality of the ICs. In practice, however, most test programs don't detect all possible defects.

In addition, because of the large number of potential defects, not all of the defects are even modeled. In the case of the stuck-at model, for example, only shorts from the input and output of gates to power or ground are modeled. So even 100% stuck-at fault coverage doesn't guarantee that defects like shorted FETs or bridging shorts between signal lines won't escape detection.

Because I_{DDQ} testing (both types) identifies defects by observing power-supply current rather than propagating a fault to the output test points, shorter test patterns (A = 1, B = 1) can be used. In the example, a 0 at output Z_1 in the presence of a short causes current to flow from the power supply to ground *(Fig. 2)*. A defect-free CMOS gate won't see a quiescent current flow.

The test program generation task now is much simpler; only fault-activation patterns need to be generated. Test patterns to propagate the faulty behavior to output aren't required for I_{DDQ} testing. What's more, designers find that fault activation is similar to logic verification, and the simulation patterns used for verification are quite effective at achieving high-fault coverage with I_{DDQ} testing.

A comparison of typical fault coverages achieved using conventional (voltage) testing and current testing with the same test patterns shows that current testing produces much higher fault coverage because it doesn't require fault propagation *(Table 1)*. This assumes 100% node toggle and observability with I_{DDQ} measurements on all vectors. In general, the fault coverage achieved with current testing is roughly the same as the toggle coverage. In toggle testing, the test vectors must make the existing logic level change to the complement.

Another advantage of DFT and non-DFT I_{DDQ} testing is that they're able to find defects left undetected by the many voltage detection techniques which rely exclusively on stuck-at fault models. Stuck-at models assume that every defect will cause the input or output of a gate to behave as if it's shorted to power (stuck-at-1) or to ground (stuck-at-0). This assumption was fairly accurate for TTL and ECL. However, many defects in CMOS ICs don't cause stuck-at behavior. Two examples are a short between two signal lines and an open contact on a FET *(Fig. 3)*.

I_{DDQ} testing detects many of these defects that escape stuck-at-testing. For example, to detect the short in the aforementioned example, complementary signal values are generated at the two ends of the suspected short *(Fig. 4a)*. A quiescent current flows through the power supply when a short exists.

The detection of opens is more complicated. Here, the applied test pattern causes a net to float. In the example open, the test pattern (A = 0, B = 1) turns off transistors P_2 and N_1 *(Fig. 4b)*. If transistor P_1 is open due to a defect, the output floats.

Initially, the voltage at the output stays at 1 or 0, depending upon the charge stored on the output capacitance. However, if enough time elapses, leakage currents in reverse-biased FET junctions cause the output voltage to drift to an intermediate value between 1 and 0. When that happens, the logic gates controlled by the floating signal start to conduct dc current, causing an I_{DDQ} test

TABLE 1: EXAMPLE IDDQ FAULT COVERAGES

Design style	Number of gates	Voltage test fault coverage	I_{DDQ} test fault coverage
Asynchronous	47.8 k	71%	98%
Synchronous	54.7 k	82%	99%
Asynchronous	52.1 k	N/A	97.2%
Asynchronous	46.8 k	65%	97.9%
Asynchronous	22.2 k	52%	96.1%

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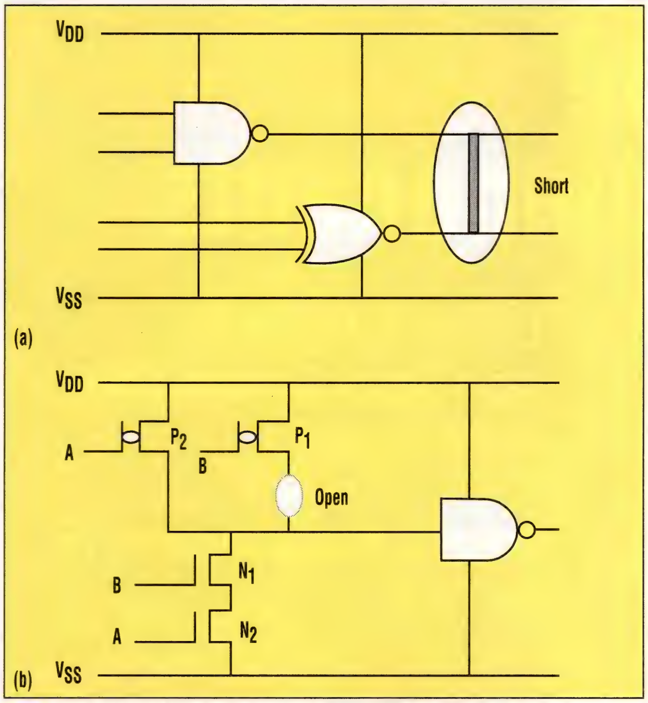
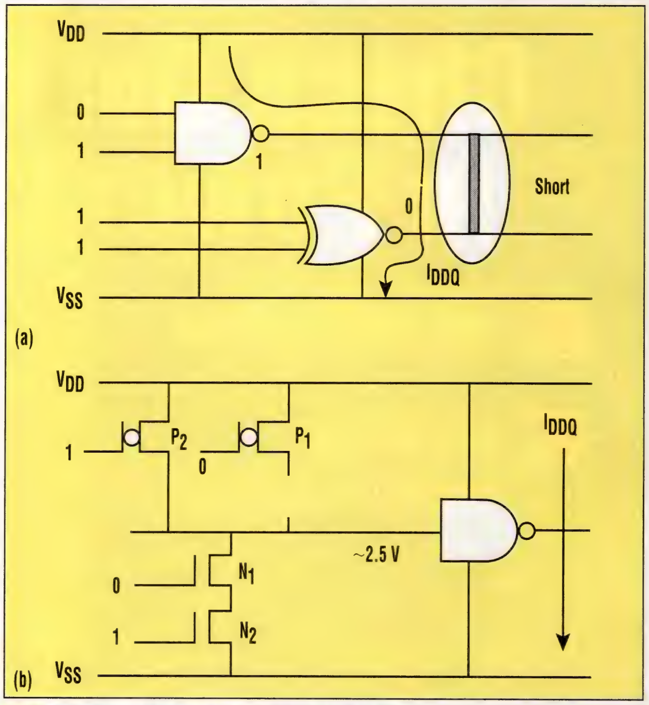


3. A SHORT BETWEEN TWO SIGNAL lines (a) and an open contact on a FET (b) are two examples of defects that conventional testing are unable to detect. That's because they don't create stuck-at faults, and voltage detection techniques rely on stuck-at fault models.



4. DETECTING THE SHORT between two signal lines can be done by generating complementary signal values on the two lines (a). In the case of open transistor contacts, the designer can apply a test pattern that causes a net to float (b), although this is not a very predictable method of detecting opens.

failure. How much time is needed for sufficient I_{DDQ} to develop depends on the node's capacitance, the leakage current, and the size and threshold voltages of the FETs being driven by the floating node.

DETECT LEAKAGE CURRENT

I_{DDQ} testing also can detect small leakage currents that are reliability concerns. For example, excessive gate leakage (current flowing through the gate oxide to the substrate) may not cause a functional defect, but could mean long-term reliability problems. I_{DDQ} measurements detect these types of defects.

Several experiments have confirmed the efficiency of current testing for finding faults left undetected by stuck-at testing. The results show that defect levels were reduced up to 11% by supplementing functional test with I_{DDQ} testing *(Table 2)*. Interestingly, the last two examples involved full-scan designs, which also benefited significantly from I_{DDQ} testing.

Non-DFT I_{DDQ} testing continues to gain interest, because it provides a relatively easy and cost-effective way to enhance circuit quality without area, performance, or power overhead. Successful use of non-DFT I_{DDQ} testing requires several steps.

The first step is to start with functional patterns that are formatted for tester use. To minimize test time, the designer should establish a minimum set of "best" I_{DDQ} test vectors selected from the set of functional patterns. This reduction is achieved by fault-simulating the functional set patterns and picking those that can detect the maximum number of defects with the fewest vectors.

These test vectors must then be checked to make sure that they don't create I_{DDQ} test hazards, which could cause many good devices to fail on the tester. The checks should include full-timing simulation to avoid timing problems and race conditions. In addition, test vectors must be screened for valid dc current states. That is, certain circuit constructs can cause a dc current without a manufacturing defect. Such constructs include tristate buses, floating nodes, certain RAM sense-amplifier circuits, pull-up or pull-down resistors on I/O pins, and internal bus holders. Because a tester can't decide whether a high current is caused by a manufacturing defect or a valid current state, any test vector that creates a valid dc current must be eliminated from the I_{DDQ} test.

Other valid design conditions that should be avoided by the vector selection software for non-DFT I_{DDQ} testing include bus conflict and potential bus conflict, as well as floating bus and

TABLE 2: HOW ADDING IDDQ TESTING CAN REDUCE DEFECTS

Company	Devices tested	Failed functional test	Failed functional and I_{DDQ} test	Defect level reduction with I_{DDQ} test
Philips	7000	1490	1511	0.3%
National	12,000	N/A	N/A	11%
Mitsubishi	400	261	285	6%
Storage Technology*	> 15 lots	N/A	N/A	5%
Hewlett-Packard*	26,415	2991	4349	6%

*Full-scan designs.

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TABLE 3: TYPICAL PMU SETTLING TIMES

Manufacturer	Model	Settling time*	Maximum number of PMUs
Advantest	T3313	3 ms	8
Advantest	T3323	3 ms	16
Advantest	T33new	3 ms 55 µs (with I_{DDQ} option)	16
Credence	ASIX-2	10 ms	1
MCT	2020	16 ms	per pin
MegaTest	Polaris	2 ms	per pin
Sentry	S10	5 ms	1
Sentry	S21	5 ms	4
LTX/Trillium	ArrayMaster	0.3 ms	per pin

*For the 100-to-800-µA range typically used for I_{DDQ} measurements.

TABLE 4: RESOLUTION VS. SETTLING TIME

Manufacturer	Model	Current ranges	Settling time (to 1% of full scale)
Advantest	T3323	800 nA	50 ms
		8 µA	10 ms
		80 µA	4 ms
		800 µA and above	3 ms
MegaTest	Polaris	40 nA	40 ms
		400 nA	4 ms
		100 µA and above	2 ms
LTX/Trillium	ArrayMaster	33 pA	330 ms
		3.3 nA	33 ms
		33 nA	3.3 ms
		1 µA	0.3 ms

potential floating bus. The software also should be able to model state-dependent current-draining cells, such as RAM cells or PLLs, and be capable of avoiding those vectors that cause static current flow from V_{DD} to V_{SS}.

Another important aspect of non-DFT I_{DDQ} testing is the use of complete fault models for fault simulation and test vector selection. One of the main advantages of I_{DDQ} testing is its ability to detect many types of shorts and opens. To select the best test vectors, the designer should fault simulate each vector with comprehensive fault models, which include transistor shorts and signal-bridging defects.

Before completing the testing, the designer also should create a fault dictionary to help diagnose failing devices. The fault dictionary lists the defects detected for the first time by each vector. All defects detected by the test vectors must be listed. If the fault dictionary contains only a subset of the defects uncovered—stuck-at faults for example—it won't help in diagnosing any other faults.

Non-DFT I_{DDQ} software solutions, such as CurrenTest developed by CrossCheck Technology, analyze the net list for the aforementioned conditions and use simulation techniques with accurate logic and timing models to identify the "invalid" circuit conditions from the user's functional vector set. The software supports standard Verilog net lists, logic models, and waveforms. CurrenTest selects a small number of "quiet" vectors for I_{DDQ} measurements. The selection process employs transistor and net-level models to analyze each of these vectors for the highest possible fault coverage.

NO DFT STRUCTURES

Because the software works with user-provided functional vectors, it doesn't require any DFT structures like scan or embedded grid structures. Therefore, it imposes no silicon-area, performance, or power overhead. In addition, the software doesn't intrude in the normal design process and can only be used to increase the quality of functional vector sets for ICs that are already in production.

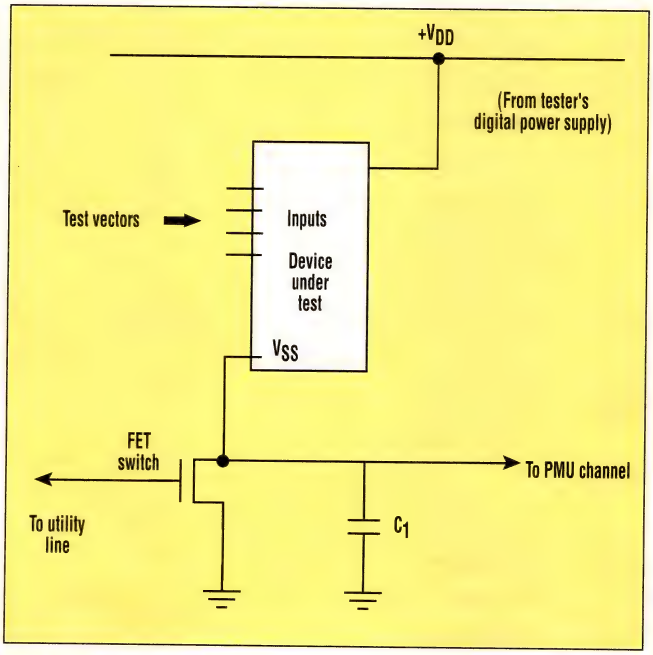
DFT-based and non-DFT I_{DDQ} testing are effective ways to enhance the quality of CMOS ICs. However, both also have several limitations that must be kept in mind. The two most important of these are the signal-to-noise ratio and the test time.

To keep good devices from failing during I_{DDQ} testing, a good signal-to-noise ratio is needed. The signal is the dc current flow caused by a defect. If the defect is a short to the power supply or between two nets, the signal could be several hundred microamperes or even a few milliamperes. However, some defects will cause a much smaller signal.

The noise current is caused by the valid leakage current through the reverse-biased junctions in each transistor on the IC. This leakage current varies with changes in process, temperature, and voltage. In addition, current transients caused by switching can have excessive time constraints approaching several milliseconds. And any noise on the power supply or input signals also may cause current to flow through the device.

For example, a 50-mV noise on the ground can cause 5 to 10 µA of noise in moderately dense ICs. As the number of transistors on a chip increases, the noise continues to build. At very high-gate counts, the noise level could become so high that it masks defects.

The other significant limitation is the long time it takes to make a measurement. Enough time should be allowed for the power-supply transient currents to diminish and for the floating nodes



5. IN THE ACTUAL TEST SETUP for I_{DDQ} testing, the tester's parametric measurement unit makes the measurement in the device's V_{SS} path.

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to drift sufficiently to cause a current flow. For example, a floating node with 1-pF capacitance could take over 50 ms to change from 5 V to 3 V.

The economics of testing limits the time that can be spent on one measurement as well as the number of measurements that can be made. Typically, 1 second of test time is considered excessive. Under such constraints, the fault coverage obtained by I_{DDQ} testing on specifically open faults can be reduced substantially. Also, there are many opens, such as power-supply or drain-contact opens, that may not be detected at all.

Unfortunately, an I_{DDQ} test gives no hint as to where the problem is on a failed IC. It could be one of millions of possible manufacturing defects, or even a bad test vector or design error. Diagnosing failures can be a very difficult task. Liquid-crystal films or secondary electron emissions are sometimes used to locate the point of current leakage. Therefore, it's important that test vectors be simulated with full-timing models and checked to ensure they won't trigger design conditions, such as floating tristate buses, that cause dc current flow. Extensive research is being conducted to improve the detection of these types of failures.

The effectiveness of an I_{DDQ} test depends on the capabilities of the ATE being used. In the early 1970s, all production ATE systems had one precision measurement unit (PMU) for I_{DDQ} measurements. In the late 1980s, leading ATE vendors started offering per-pin PMU architectures, which allowed test and product engineers to monitor I_{DDQ} as a power-consumption pass/fail screen for CMOS devices.

The ATE time required using a PMU approach depends on the measurement resolution of the power supplies. Typical settling times of commercial testers run from under 1 ms to 16 ms *(Table 3)*. For a specific tester, a higher resolution means a longer settling time for PMUs *(Table 4)*.

While the device under test (DUT) is in a particular static state, the PMU makes the measurement in the device's V_{SS} path *(Fig. 5)*. A typical algorithm for the test control program includes the following steps, which are taken from Hewlett-Packard Application Note 398-3, "Measurement of I_{DDQ} with the HP 82000":

1. Switch the FET "on" by applying 5 V to its gate. This connects V_{SS} directly to ground while the tester runs the functional vectors.
2. Set the PMU to the correct range (20 µA, 200 µA or 2 mA) with a force voltage of 0.0 V.
3. Connect DUT to the pin electronics and PMU.
4. Execute test vectors that put the DUT into the "quiet" state.
5. Connect the PMU to the ground path by switching the FET "off."
6. Wait the PMU's settling time.
7. Read the PMU current.
8. Repeat the entire sequence for the next chosen vector.

Some testers offer special I_{DDQ} measurement units to speed up these steps. In one such tester, the measurement unit is mounted on the test head, which keeps it close to the DUT and helps reduce noise and improve repeatability. Its 12-bit analog-to-digital converter has a current resolution of 4 nA.

Recently, the Quality Test Actions Group proposed an off-chip current-monitoring device that can be used on the DUT board. This small-outline, 8-pin packaged chip allows the tester to monitor I_{DDQ} at a speed of 50 kHz. The group, which was formed at last year's International Test Conference in Baltimore, will present data on using this approach at the 1994 ITC in Washington (Oct. 3-5).

The best way to benefit from I_{DDQ} testing is to use it as part of an overall functional test strategy, where quiescent power-supply current is measured on selected functional test vectors. By incorporating I_{DDQ} testing into the DFT process, engineers will see a substantial improvement in the quality of their functional vector sets. ☐

Vic Kulkarni, vice president of marketing and strategic programs at CrossCheck Technology, received his bachelor of technology in electrical engineering from the Indian Institute of Technology in Bombay and his MSEE in solid-state electronics from the University of Cincinnati, Ohio.

HOW VALUABLE?	CIRCLE
HIGHLY	557
MODERATELY	558
SLIGHTLY	559

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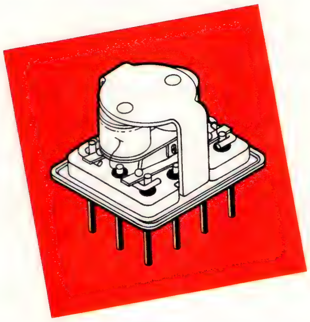

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READER SERVICE 133

ELECTRONIC DESIGN QUICKLOOK

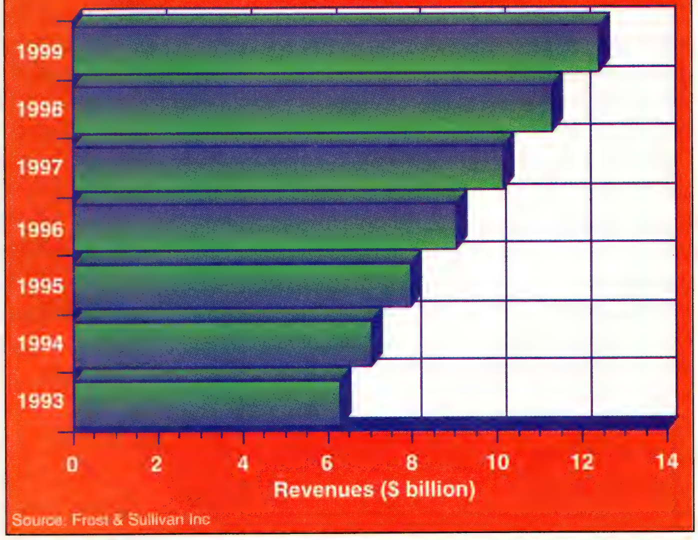
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

The worldwide market for semiconductor production equipment is growing at a robust 12% compound annual rate, driven by increasing demand for new electronic products that semiconductors make possible. The market for such equipment will nearly double from $6.3 billion in 1993 to $12.4 billion by 1999, according to Frost & Sullivan Inc. The Mountain View, Calif., market researchers break out percentages of worldwide market revenues last year as follows: vapor deposition, 21%; in 1993; test equipment, 19%, microlithography and etching equipment, 18% each; diffusion furnaces, 5%; ion implantation equipment, 4%; and others, 15%.

The market researchers pinpoint an emerging economic recovery as sparking 13% growth in the 1995-6 period. Trends to watch include dry-etch gaining popularity over wet-etch and vertical diffusion furnaces displacing horizontal furnaces. The researchers say high-current ion implementation equipment continues to be the most popular type. Growth is most rapid outside Japan, the U. S., and Europe. particularly in the Pacific Rim, where South Korea represents a growing market.

MARKET ROBUST FOR SEMICONDUCTOR PRODUCTION EQUIPMENT



Source: Frost & Sullivan Inc

TIPS ON INVESTING

As markets become more volatile, engineers with investments seek ways to reduce risk and maintain returns. A strategy you can use to get even better performance from your stock portfolio is through an automatic dividend reinvestment program. When you reinvest dividends, you use these earnings to buy additional shares of stocks. As a result, the number of shares you hold will grow dramatically over time—and so may the potential return on your stock portfolio. Consider this: From Jan. 1, 1978 to March 31, 1993 the Standard & Poor's Index, a popular unmanaged index of widely held stocks, grew more than 400%. But with dividends reinvested in additional shares, those returns jumped to 851% (source: Standard & Poor's Corp.).

Here's an example: Let's say you own 1,000 shares of Company G stock and the current market price is $50. If the stock pays a $1 dividend annually, you've earned $1,000 to reinvest in the market. Your dividends would buy an additional 20 shares of Company G stock (assuming the stock price stays at $50 per share). Your holdings in Company G would increase to 1,020 shares while dividend earnings ($1 dividend annually) would grow to $1,020.

As you know, stock prices can move up or down at any time. However, a simple but effective way to take advantage of stock fluctuations is through dollar-cost averaging. By investing equal amounts of money on a regular basis, you buy more shares when prices are lower and fewer shares when prices are higher. Although dollar-cost averaging doesn't guarantee you a profit or protect you from loss in declining markets, it is an easy, time-tested way to use market fluctuations to your advantage. If you reinvest dividends on a regular basis, you are dollar-cost averaging.

The difficulty in reinvesting dividends from your stock holdings is that in many cases you have to contact each issuing company and join its dividend reinvestment program. But there's an easier way. A few full-service brokerage firms now offer automatic dividend reinvestment services that allow you to reinvest dividends on stocks in your account. Many times you can enroll by making a phone call.

Enrolling in a dividend reinvestment program is usually an easy process. If you're thinking about joining one, here are some questions you should ask before you sign up:

- Does the firm offer dividend reinvestment for a wide range of stocks from all the major exchanges?
- Does the company provide a comprehensive statement, reporting all account activity, plus tax summaries?
- What fees are charged for dividend reinvestment services?
- Does the company offer discounts on large purchases or free reinvestment on certain accounts, like IRAs?
- Does the firm pass on any discounts received when reinvesting in stocks of companies offering a discount?

Henry Wiesel, financial consultant, investment counselor, and pension coordinator, can be reached c/o Smith Barney, P. O. Box 8729, Red Bank, NJ 07702; (800) 631-2221.

HOT PC PRODUCTS

The UltraStat installs on any computer and continually drains static from the system and the user. The $59.95 device incorporates a synchronized dual resistance circuit card and a unique custom liquid crystal display. The user can see a custom LCD figure called Ernie get zapped before static zaps the computer. Warranted for five years, the UltraStat has a 30-day free trial. Contact UltraStat Inc., P. O. Box 791, Colorado City, CO 91019; (800) 460-7828; fax (719) 676-4012. CIRCLE 460

Computer users spend up to 10% of their time searching for files; DOS's restriction to eight-character filenames is at least partly responsible. Sherlock version 2.0 file-finding and management software for Windows 3.1 enables users to find files on individual systems or across networks by using 254 character file descriptions and other file-access fields. Sherlock extends the Windows filing environment by seamlessly replacing the Windows Save and Open dialog boxes with access to Sherlock's file access cards and 254-character file descriptions. The product also has a visual filing environment with familiar screen icons; network stations look like offices; drives are file cabinets; and subdirectories and resemble files drawers and folders. Sherlock also allows the user to automatically launch applications for the selected document. Sherlock 2.0 is $139 for single users and $695 for a 10-station LAN pack. Contact 2010 Software Corp., 611 Route 46 W, Hasbrouck Heights, NJ 07604; (201) 288-7100; fax -7274. CIRCLE 461

An upgrade to QAPlus/Win 6.0, which gives online support in troubleshooting PC problems, has several new diagnostic features. With a single click, a user can run some basic tests to find the cause of the problem; if unable to solve the problem, a user can click on an icon and type a description of the problem. The user can choose from various options, including talking to a support technician or receiving a response by e-mail or fax. QAPlus/WIN then automatically connects to DiagSoft's support center by modem. Support hours are 8 am to 5 pm, Monday through Friday, Pacific Standard Time, but a user can upload an inquiry at any time. List price for version 6 is $99.96; upgrades are $39.95. Contact DiagSoft, 5615 Scotts Valley Dr., Suite 140, Scotts Valley, CA 95066; (408) 438-8247; fax -7113. CIRCLE 462

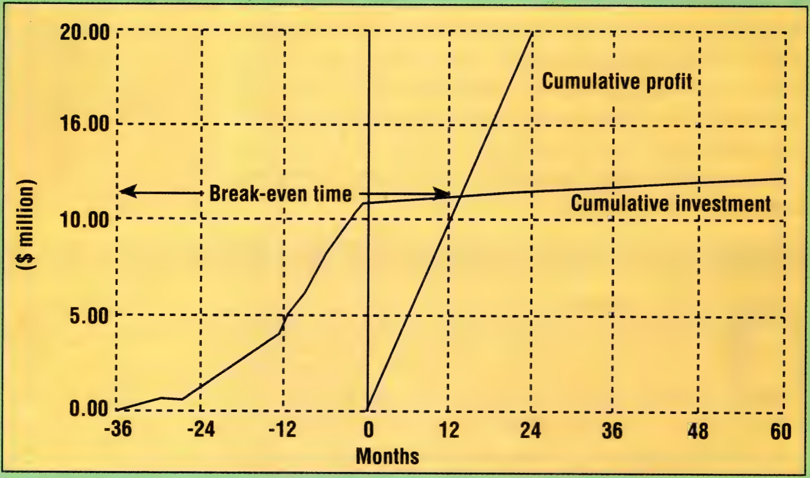
KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

We want a competitive break-even time, a new-product time line that gives us a distinct business advantage. BET is the cross-functional measure of new product development success. To make the idea work in business, engineering must produce the right product, in the right time frame, at competitive product and development costs; manufacturing must build the product economically at volume while meeting customer delivery and quality requirements; and marketing must sell the product profitably while generating sufficient order volume to satisfy an organization's financial needs. Everybody contributes to the measure and shares in new product success or failure—measuring BET helps you make better decisions.

By definition,. BET measures investments and profits. On the investment side, you'll want to know the money spent on marketing, manufacturing, engineering, engineering support, tooling, facilities, capital, and other items. Profit computation forces understanding of product manufacturing costs, sustaining engineering, costs of sales, costs of distribution, discount mechanisms, and the like. Diversity of financial information lies within the concept. Getting accurate, timely, simplified data that is easily charted makes the concept work. If you have to work too hard, for too long, developing numbers that mean little to anyone, the BET notion fails. To implement the concept, form a cross-functionally team tasked with installing the BET metric. Do not make installation the responsibility of one person or project manager—the magnitude of work renders an individual ineffective. If you do not now measure break-even time, expect your team to snag a few dead fish as they troll murky financial waters. Making BET measurement and presentation functional requires diligence, talent, and perseverance on the part of your team and your organization. Preliminary success may be visible in a few months; full use throughout the organization may require an extended period. Along the way, your organization identifies the tools needed for automated generation of the break-even graph *(see the figure)*.



Ron Kmetovicz's The One-Minute Time to Market Self Assessment, which identifies five key behavioral patterns exhibited by fast-moving new product development organizations, is available free to the readers of Electronic Design by contacting Time to Market at the address above.

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MY VIEW

...Gerontophobia

BY FRANK J. BURGE
Director of Market Development for Electronic Design

My friend Buford Barr gave a talk on age diversity and generation wars at a recent Business Marketing Association lunch in Santa Clara, Calif. His presentation was based in part on his survey of the association's membership. Buford, a transplanted Texan, teaches part-time at San Jose State and Santa Clara University and has a full time job at Actel in Sunnyvale, where he is director of communications. My barber tells me Barr is one of the smartest Texans he's ever met, and my barber ought to know: He's from Brooklyn. Buford wondered if any of the members of the audience have gerontophobia—that is, a fear of aging and a prejudice against the old.

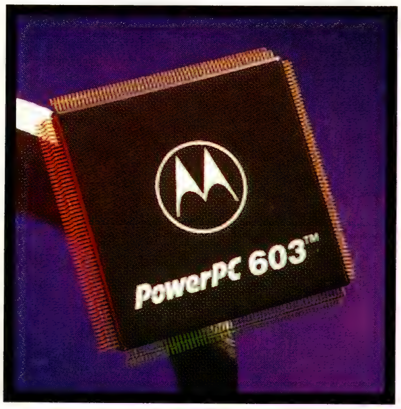
As an almost-old geezer myself, I certainly don't have any prejudice against my older colleagues mostly because there are so few of them around. But I must admit there are times I get a bit annoyed at the aging process—now what was it I was talking about? A number of studies have shown that in a wide variety of fields, people are most productive in early adulthood and then undergo a steady decline. Yet there is no apparent physical reason for this. It may be that as we enter middle age we either become distracted by new responsibilities or are lulled into complacency by a management position. We may become more conservative as a result of having more to lose and mounting responsibilities.

What else can we say about productivity? Barr points out that over 100 years ago, psychologist G. M. Beard pioneered the idea that productivity is a combination of enthusiasm and experience. Enthusiasm is abundant in the beginning of one's career, then declines gradually. Experience, by contrast, starts from zero and grows over the course of a career. Enthusiasm without experience results in original but often unfocused effort, while experience without enthusiasm results in uninspired work. But in Beard's time, the personal computer was only a gleam in Steve Job's great-grandfather's eye.

Younger folks are more computer-literate than most of the 50+ generation; that gives them an advantage. Still many of my contemporaries argue that e-mail has replaced walking down the hall for a face-to-face chat and that eventually we'll all become strangers.

So why all this talk lately about the generation wars? From Barr's perch, it seems that many of our middle-aged colleagues are running scared and rightly so. Downsizing has devastated the middle-management ranks at a time when managers have finally built a comfortable life style, have a hefty mortgage and college tuition bills that would choke a plow horse. And those who are still employed are looking over their shoulder, wondering if they will be next. And their already fragile careers are further threatened by highly educated, computer proficient, aggressive young professionals who don't want to wait half a career to get the boss's job. Conflict city.

Moreover, the conflict is getting worse, just when companies need a hefty increase in productivity. Bigger whips and louder threats seldom achieve the desired results, though. In Buford Barr's view, the secret in doing more with less means encouraging and rewarding individuals to work together. But dissension in the ranks, now driven by the generation wars, makes teamwork difficult if not impossible. Why should I share my experience with one of those young turks who is after my job? Buford concluded his remarks with a list of ways companies can turn age diversity into an asset. I am sure he would be happy to share his thoughts with you; call him at (408) 739-1010. If an old geezer answers, hang up.



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READER SERVICE 130

CIRCLE 520

SPICE MODELS NORTON-INPUT AMP

JIM HONEA
Aerospace Controls Corp., 6310 Lindsey Rd., Little Rock, AR 72206.

The versatile LM359 dual Norton-input amplifier can be modeled using a Spice subcircuit *(see the listing and Fig. 1)*. Just as with the actual device, key amplifier parameters are programmed using external resistors or current sources. Features modeled by the subcircuit include the input current mirror, dc gain, bandwidth, slew rate, output saturation voltages, and dynamic and quiescent supply currents.

Looking at the diagram, the currents that program the amplifier are those flowing out of node 1 ($I_{set\ out}$) and into node 8 ($I_{set\ in}$). $I_{set\ in}$ controls bandwidth, slew rate, and input bias current by setting the bias current in the gain stage, which consists of F1 and Q3. To get the bandwidth, but not the dc gain, of the gain stage to be a function of bias current, the Early voltage (V_{AF}) of Q3 simply is set to an appropriate finite value (103 V in this case). The LM359 actually has a cascode gain stage, but with Spice, cascode performance can be achieved from a simple common-emitter amplifier by setting the collector-base capacitance to zero. The output-stage bias current is set to 10 times $I_{set\ out}$.

The subcircuit as listed provides only one amplifier. To model both sides of the LM359, everything but the bias stage should be duplicated. Then the node numbers in the duplicate section must be changed, and the interface nodes to the .SUBCKT line added.

A word of advice: The LM359, like other amplifiers, is sensitive to external parasitic impedances, especially when it's programmed for high-speed operation. If parasitic elements aren't included in the Spice net list, Spice will (correctly) predict incorrect performance for the circuit. Particularly important parasitic elements are capacitance from the inverting input (node 6) to ground, from the compensation pin (node 3) to ground, and from the output to the inverting input (node 2 to node 6, i.e., feedback capacitance). Values of capacitance in the 3-to-5-pF range at nodes 3 and 6, and the 0.2-to-0.3-pF range from node 2 to 6, are probably realistic. For starters, the subcircuit already includes 1 pF of package capacitance at pin 6.

To illustrate this point, consider a comparison of the actual and predicted step response for a unity-gain inverting amplifier featuring a 270-μA

EDITORIAL CALL: WANTED—MORE IDEAS FOR DESIGN

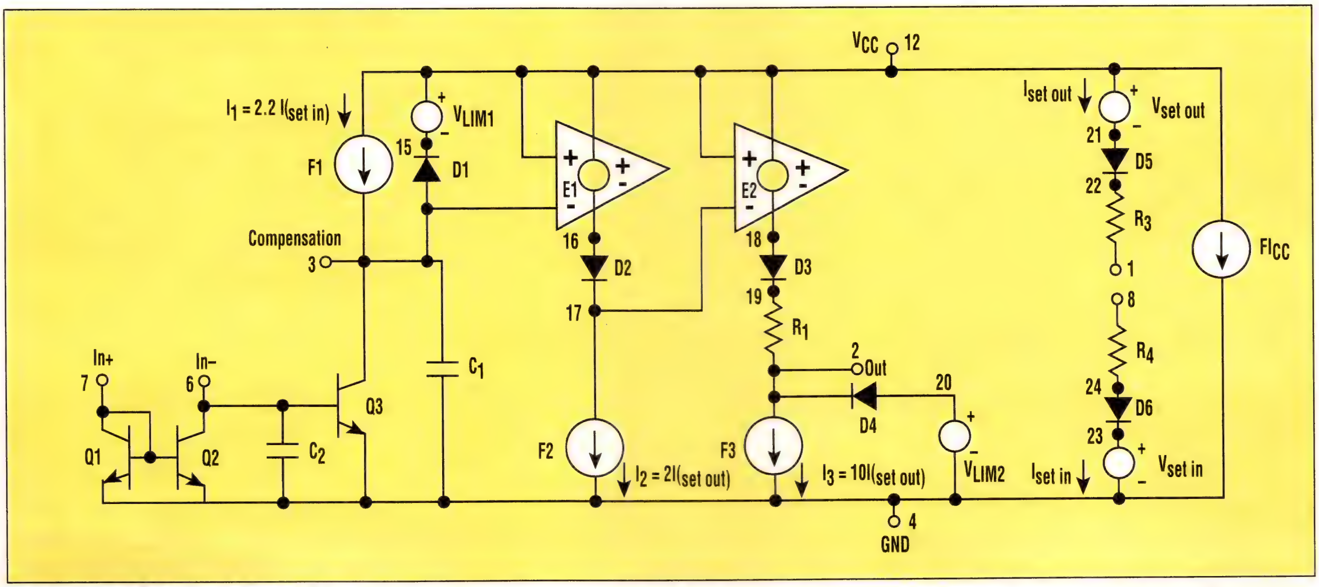
We recently expanded the Ideas for Design section to include more items in each issue. To continue this expanded section, however, we will need a steady flow of ideas.

We depend on our readers to keep this section going. This is an opportunity for our reader-engineers to gain recognition for, as well as share, their innovative ideas with other engineers throughout the world. Issue after issue, Ideas for Design is voted highest on the "Of Interest" scale in our reader surveys. We pay $100 for each Idea for Design we publish, and the IFD voted best of the issue brings the author an additional $150.

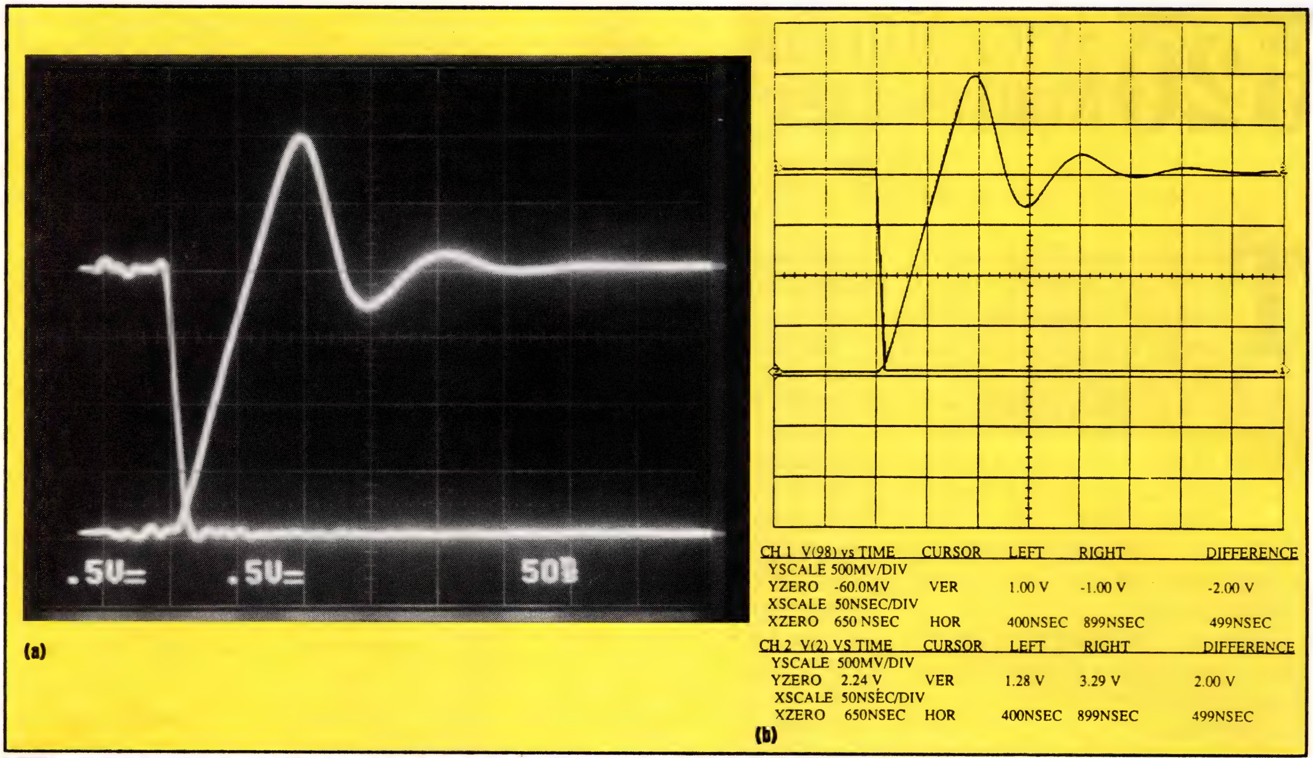
Submissions to the Ideas for Design section should be about one typewritten page of text, with one or two circuit diagrams or block diagrams. They should represent the author's original work, be tested to prove they actually work, and not have been published previously. Please include telephone and fax numbers, if available.

Send your Ideas for Design to:

Ideas for Design Editor
Electronic Design
611 Route 46 West
Hasbrouck Heights, N.J. 07604
Fax: 201-393-0204



1. THIS SPICE MODEL of National Semiconductor's LM359 makes it possible to control key amplifier parameters by externally setting the currents into and out of nodes 8 and 1.



```
CH 1  V(98) vs TIME      CURSOR      LEFT       RIGHT              DIFFERENCE
  YSCALE 500MV/DIV
  YZERO   -60.0MV        VER         1.00 V     -1.00 V            -2.00 V
  XSCALE  50NSEC/DIV
  XZERO   650 NSEC       HOR         400NSEC    899NSEC            499NSEC
CH 2  V(2) VS TIME       CURSOR      LEFT       RIGHT              DIFFERENCE
  YSCALE  500MV/DIV
  YZERO   2.24 V         VER         1.28 V     3.29 V             2.00 V
  XSCALE  50NSEC/DIV
  XZERO   650NSEC    HOR             400NSEC    899NSEC            499NSEC
```

2. BY INCLUDING BREADBOARD parasitics, the step response of a unity-gain inverting amplifier (a) is very close to that predicted by Spice (b).

set current *(Fig. 2)*. The simulation was only achieved when the actual parasitic capacitances on the breadboard were measured and included in the net list. By omitting various combinations of parasitic elements, Spice can be made to predict anything from critical damping to instability for this same circuit. This also demonstrates why National recommends adding compensation capacitance in low-gain applications of the LM359.☐

```
* LM359 Norton amplifier circuit
*
* connections:
* non-inverting input: 7
* inverting input: 6
* positive supply: 12
* negative supply: 4
* output: 2
* compensation: 3
* Iset out: 1
* Iset in: 8
*
.SUBCKT LM359 7 6 12 4 2 3 1 8
*
Q1 7 7 4 QMOD 2
Q2 6 7 4 QMOD 2
Q3 3 6 4 QMOD
F1 12 3 VSETIN 2.2
C2 6 0 1PF
VLIM1 12 15 0.7V
D1 3 15 DMOD
C1 3 4 14PF
E1 12 16 12 3 1
D2 16 17 DMOD
F2 17 4 VSETOUT 2
E2 12 18 12 17 1
D3 18 19 DMOD 5
R1 19 2 10
F3 2 4 VSETOUT 10
VLIM2 20 4 0.7V
D4 20 2 DMOD 5
FICC 12 4 POLY(2) VSETIN VSETOUT 0 2 1
*
* bias section
*
VSETOUT 12 21 0V
D5 21 22 DMOD
R3 22 1 500
VSETIN 23 4 0V
D6 24 23 DMOD
R4 8 24 500
*
.MODEL QMOD NPN BF=150 VAF=103 IS=1.5E-15 CJE=1PF TF=0.35NS
.MODEL DMOD D(IS=1.5E-15)
.ENDS
```

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

IFD WINNER

IFD Winner for May 16, 1994

John Dunn, 181 Marion Avenue, Merrick, NY 11566. His idea: *"Equalize PAD Power Dissipations."*

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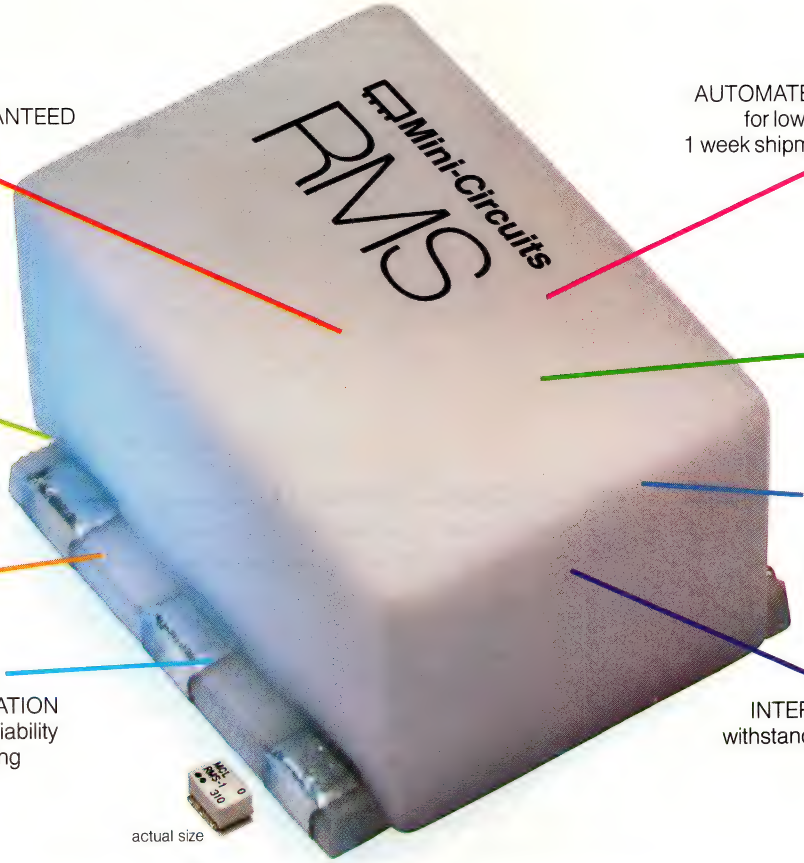

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RMS-11F	+7	350-2000	DC-400	5.5	31	30	4.95
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RMS-25MH	+13	5-2500	5-1500	7.5	32	32	7.95

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READER SERVICE 98

F166 REV. ORIG.

CIRCLE 521

PROGRAMMABLE ANALOG FILTER

JOHNNIE MOLINA
Burr-Brown Corp., Tucson, AZ 85706; (602) 746-7592.

Programmable active filters have increased in popularity over the past decade. With the advent of switched-capacitor topologies, filter parameters such as the natural frequency and filter Q can be changed simply by varying the clock frequency. This allows different filter responses to be achieved using the same hardware. But switched-capacitor filters are sampled data systems and are subject to anomalies like clock feedthrough noise and aliasing errors.

The circuit in Fig. 1 shows how an analog, digitally programmable filter can be built using a UAF42. This monolithic, state-variable active filter chip, provides a two pole filter building block with low sensitivity to external component variations. It eliminates aliasing errors and clock feed though noise common to switched-capacitor filters. Low-pass, high-pass, bandpass and notch (band-reject) outputs are available.

The circuit uses the UAF42 state-variable filter IC, two op amps, a few resistors, and two common MDACs. Capacitors aren't required because the UAF42 has on-chip 1000-pF, 0.5%-precision capacitors. The MDACs function as voltage attenuators, which influence the unity-gain bandwidth of the integrators onboard the UAF42. The filter's natural frequency, f_o, is described by the following relationships:

$f_o = (gain_{DAC})(f_{o\,max})$

where

$gain_{DAC} = X/2^n$

$f_{o\,max} = 1/(2\pi 10^{-9})(R_F)$

$R_F = R_{F1} = R_{F2}$

X = digital word at DAC inputs D1-D12

n = number of DAC bits

For example, to program a 60-Hz notch filter with the circuit shown in Fig. 1, the digital word to the MDAC is given using the above relationships:

$X=(2\pi 10^{-9})(R_F)(f_o)(2^n)$

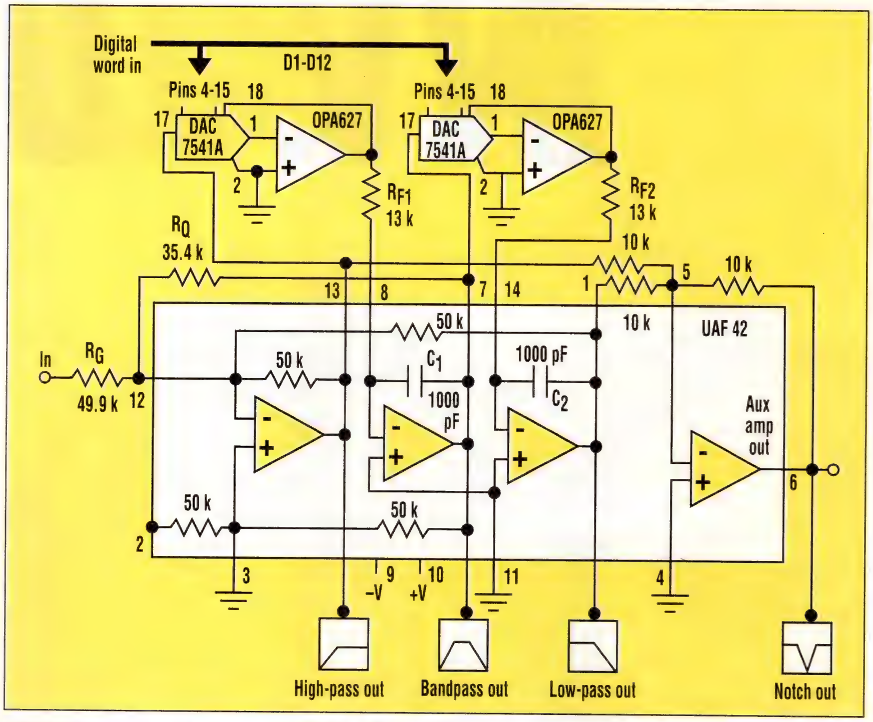
given that

$f_o=60$, $R_F=13K$, and $n=12$

then

$X=20.1$

The 12-bit digital word to the DAC should be equal to decimal 20, or 000000010100. The rounding error introduced is 0.3% (f_{notch} =59.8 Hz).



1. BUILDING THIS ANALOG, digitally programmable filter merely requires a monolithic state-variable active filter chip and a couple of garden variety MDACs. Ultimately, switching noise and aliasing are eliminated.

Note that the natural frequency f_o is equal to f_{notch}.

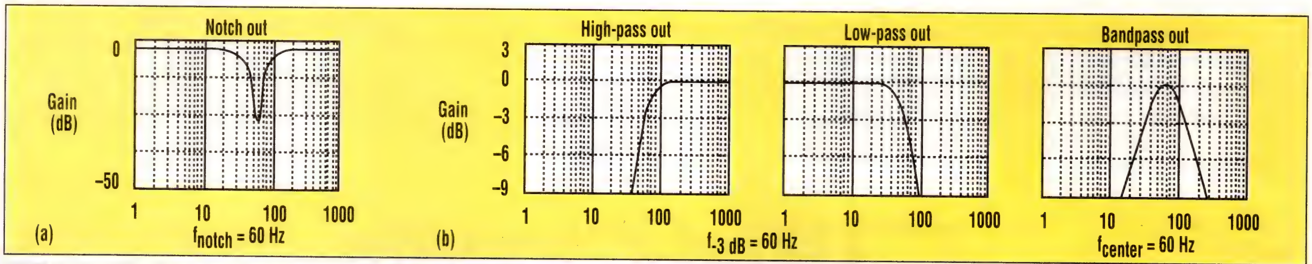
Fig. 2a shows the response seen at band reject or "Notch Out" node.

The high-pass, bandpass and low-pass outputs yield the responses shown in Fig. 2b.

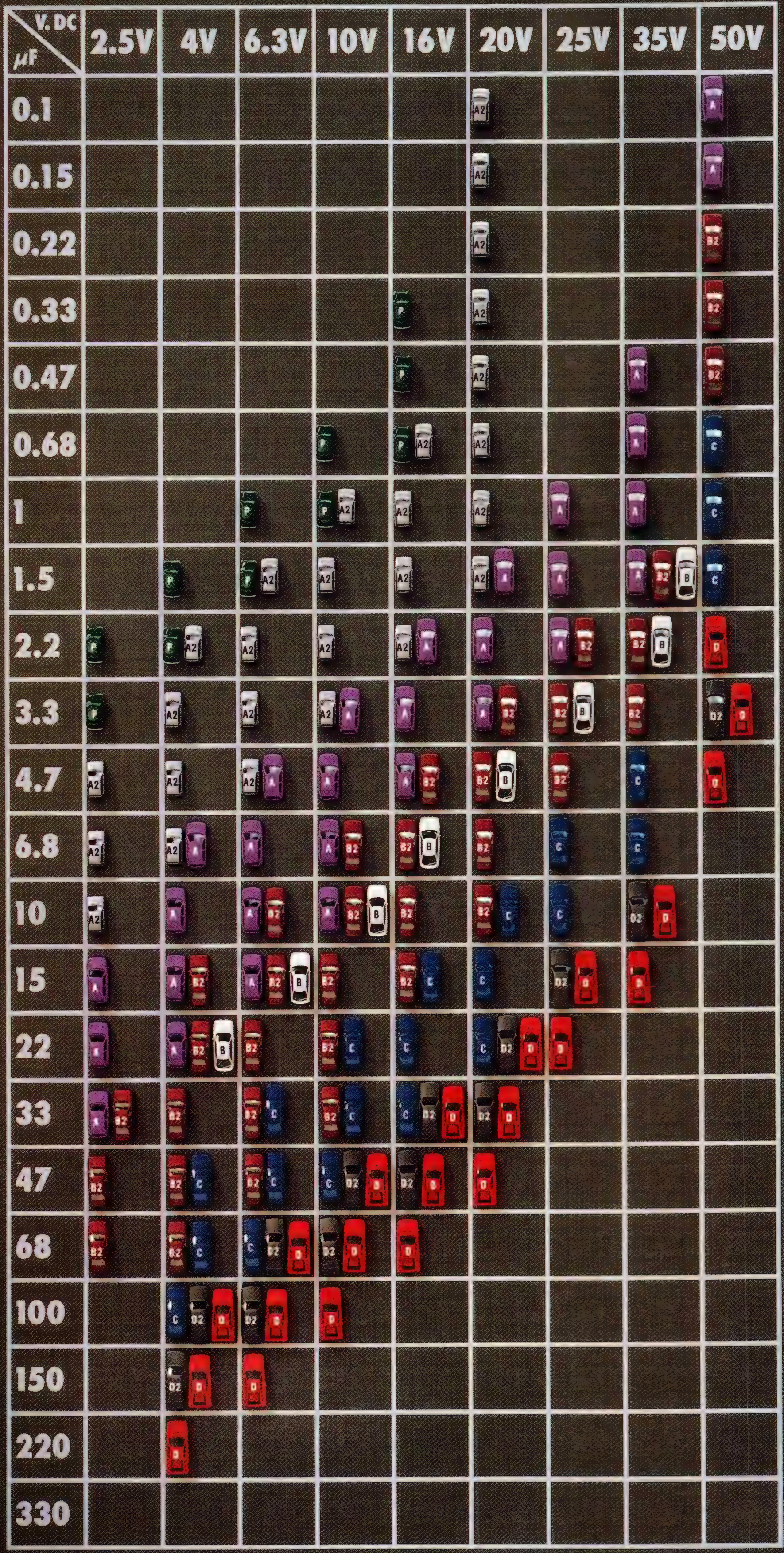
The filter in Fig. 1 is set for a Q of 0.707. This can be adjusted using the following equation:

$R_Q=(50\ k)(Q)$

Setting the filter to a Q of 0.707



2. 60-Hz RESPONSES SEEN AT THE BAND REJECT or "Notch Out" node (a) and at the high-pass, bandpass, and low-pass outputs (b) are given.



µF \ V. DC	2.5V	4V	6.3V	10V	16V	20V	25V	35V	50V
0.1						A2			A
0.15						A2			A
0.22						A2			B2
0.33					P	A2			B2
0.47					P	A2		A	B2
0.68				P	P A2	A2		A	C
1			P	P A2	A2	A2	A	A	C
1.5		P	P A2	A2	A2	A2 A	A	A B2 B	C
2.2	P	P A2	A2	A2	A2 A	A	A B2	B2 B	D
3.3	P	A2	A2	A2 A	A	A B2	B2 B	B2	D2 D
4.7	A2	A2	A2 A	A	A B2	B2 B	B2	C	D
6.8	A2	A2 A	A	A B2	B2 B	B2	C	C	
10	A2	A	A B2	A B2 B	B2	B2 C	C	D2 D	
15	A	A B2	A B2 B	B2	B2 C	C	D2 D	D	
22	A	A B2 B	B2	B2 C	C	C D2 D	D		
33	A B2	B2	B2 C	B2 C	C D2 D	D2 D			
47	B2	B2 C	B2 C	C D2 D	D2 D	D			
68	B2	B2 C	C D2 D	D2 D	D				
100		C D2 D	D2 D	D					
150		D2 D	D						
220		D							
330									

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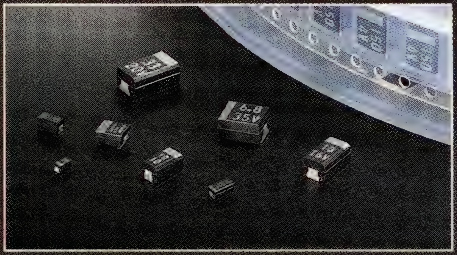
B2	3.5	2.8	1.9
B	4.7	2.6	2.1
C	6.0	3.2	2.5
D2	5.8	4.6	3.2
D	7.3	4.3	2.8



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produces second-order Butterworth responses. The Q is unaffected by natural frequency programmed by the DACs. Note that for Butterworth filters, the natural frequency also is the –3 dB (half-power point) for low-pass and high-pass responses. It's also the center frequency for bandpass filters and the notch frequency for band-reject responses.

The maximum f_o in Fig. 1 is set for 12.25 kHz. This can be adjusted using the basic equation for f_o. Set the DAC gain term equal to $(2^n–1)/2^n$ and $f_o = f_{o\,max}$, and solve for R_F.

For example, to extend the maximum f_o to 20 kHz:

$$R_F = (4095/4096)/(2\pi 10^{-9} \times 20\ \text{kHz})$$
$$= 7.96\ \text{k}$$

The maximum natural frequency obtainable for the UAF42 is 100 kHz.

The accuracy of f_o can decrease as the DAC gain decreases in an attempt to program low natural frequencies. For example, for a 12-bit DAC and maximum f_o set to 20 kHz, the resolution given one LSB change is:

$$\text{Resolution} = (f_{o\,max})(1/2^{12})$$
$$= (20\ \text{kHz})(1/4096)$$
$$= 4.9\ \text{Hz}$$

When trying to program to a low natural frequency like 12 Hz, the digital word to the DAC would be 2. Therefore:

$$f_o = (f_{o\,max})(2/4096)$$
$$= (20\ \text{kHz})(2/4096)$$
$$= 9.8\ \text{Hz}$$

This is an 18% error. Note that Resolution can be increased by reducing $f_{o\,max}$ or by using a higher-order DAC. R_F's resistive tolerance should be kept below 1% to maintain f_o error to within ±1%. The OPA627 op amps are chosen for their low offset voltage, low noise, low input bias current (FET input), and high unity-gain bandwidth (GBW=16 MHz) to maintain stability.□

IFD WINNER

IFD Winner for May 30, 1994

Michael A. Wyatt, Honeywell Inc., 13350 U.S. Highway 19, MS-931-4, Clearwater, FL 34624. His idea: *"Filter Improves Stop-Band Rejection."*

CIRCLE

522

SIMPLE BIDIRECTIONAL BUFFER DESIGN

YONGPING XIA
EBT Inc., 23600 Telo Ave., Torrance, CA 90505.

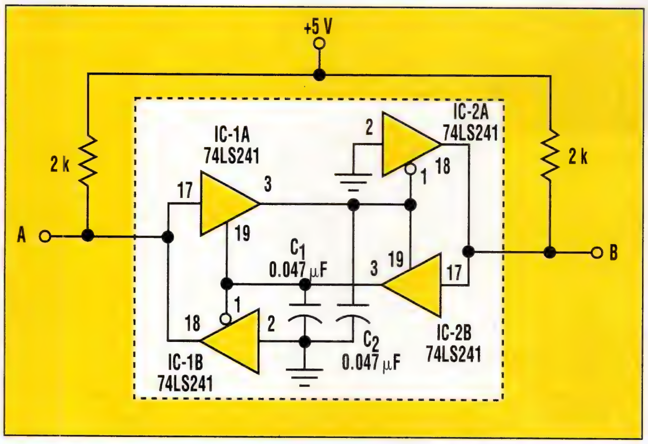
A previously published design idea (ELECTRONIC DESIGN, *Mar. 18, 1993, p. 67)* used discrete circuits to create a noninverting and nonlatching buffer. However, common ICs can do the same job in a simpler circuit, and attain higher performance.

The circuit shown in the figure uses two 74LS241s to create such a buffer. When both input/output lines are high, IC-1A and IC-2B turn on, and C_1 and C_2 are charged to high voltage. Meanwhile, IC-1B and IC-2A are off to prevent a logic "1" latch.

If input A goes low, IC-1A's output goes low, turning on IC-2A and turning off IC-2B. Thus, point B goes low and IC-2B's output becomes high impedance. Since C_1 is charged to high, it will remain charged because of the open-circuit input at IC-1's control terminals, which is equivalent to logic "1", is the TTL's circuit's nature. This will force IC-1A on and IC-1B off to prevent logic "0" latch.

C_1 and C_2 stabilize the circuit when the bus has a high capacitance load. When input A changes from low to high, it turns off IC-2A and turns on IC-2B. If input B has a high capacitance load, the voltage on input B can't change to high immediately because the pull-up resistor can only provide limited current. As a result, IC-2B's output will have a narrow negative glitch. This glitch will be absorbed if C_1 is large enough. The drawback of using a large C_1 and C_2 is a longer delay, which reduces communication rate. If C_1 and C_2 are 0.047 μF, the circuit has a 1.3-μs delay. The rate can be as high as 150 kHz if load capacitance is less than 1000 pF.

The circuit's logic "0" drive ability is –24 mA. Note that the logic "0" voltage is lower than that of the original design, which is equal to a diode forward drop plus a transistor saturation voltage.□



THIS simpler version of a previous Idea for Design can buffer bidirectional lines using just two 74LS241s.

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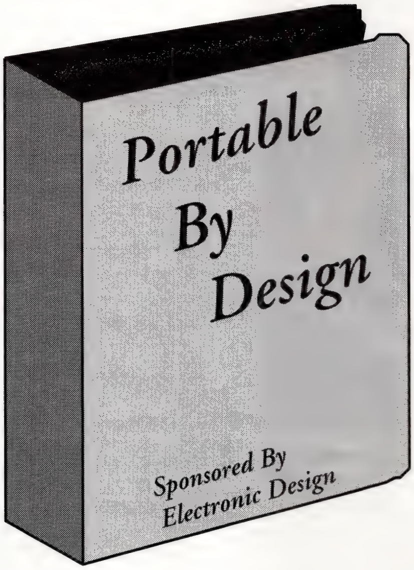

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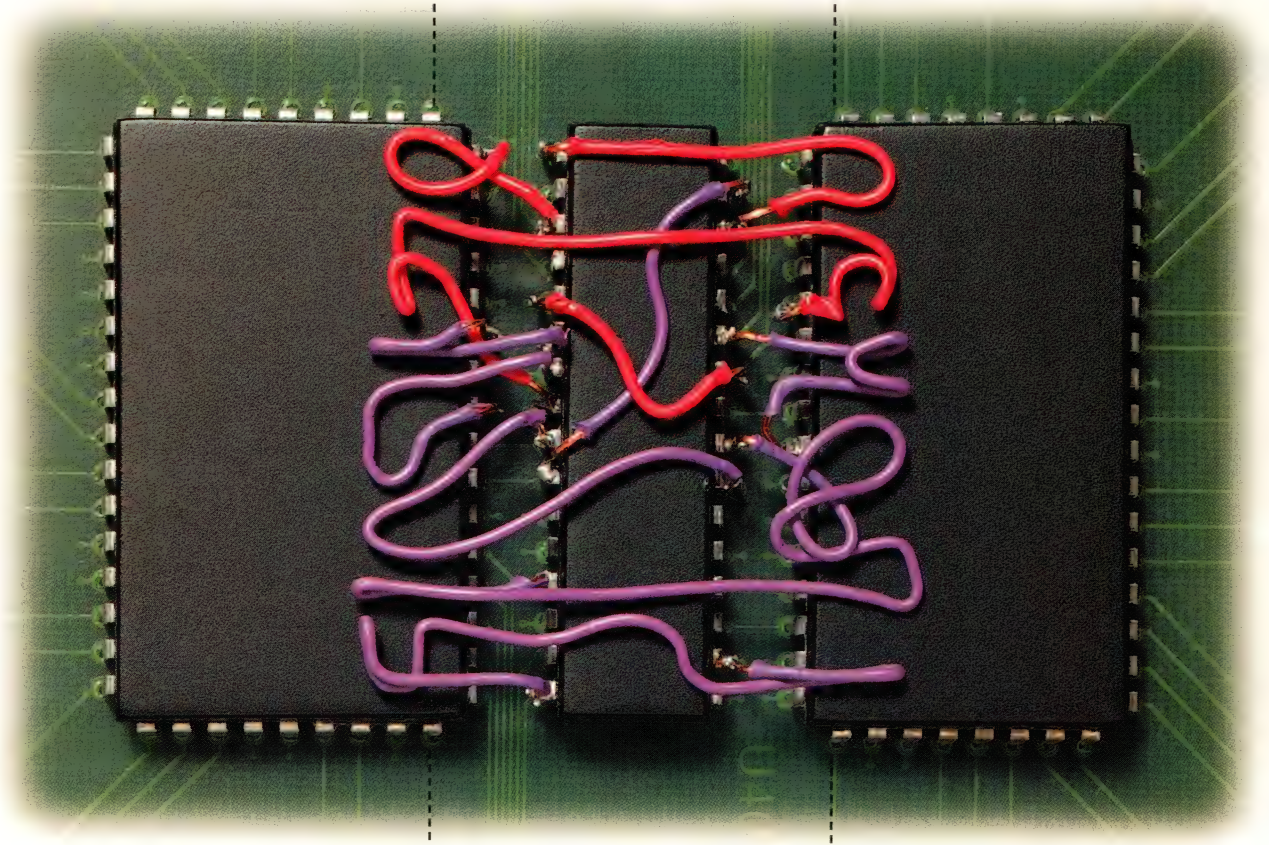

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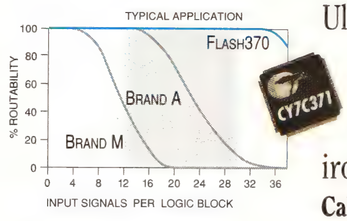

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ULTRA LOGIC

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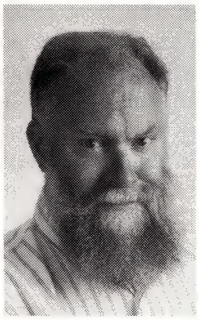
WHAT'S ALL THIS ELECTRIC CAR STUFF, ANYHOW?

A few weeks ago I read a letter (published in *EE Times*) by our old friend, Jim Hansen of New Boston, N.H. He presented several reasons why an electric car would have problems achieving great popularity, even though several states have passed laws mandating that cars that make zero pollution, must be made available, for us to buy. If an electric car is to be made efficient, it must be very light yet very strong, he observed. This typically leads to a fairly fragile structure, which is not only expensive, but, if you get into one little accident, it is liable to be bent and crumpled and not repairable. One ding and it is smashed. These will not be inexpensive cars to own, when they start having accidents.


BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Also, he observed, an electric car is made of exactly the kind of materials (high-current batteries, bus bars) that one would use to make a welder. In case of an accident, the arc-welding begins.... Not a fun place to be in an accident. Also, if the battery cases crack, there will be battery acid all over the street. Messy. And what if there is an electrical breakdown in the control computer? You might have a healthy motor, and healthy batteries, but you still couldn't get home. And in cold weather, how do you run the heater? In hot weather, are you supposed to do without air-conditioning?

I sat down and started writing to Jim. The problem of welding can be solved if suitable fuses are built into the bus-bar paths. The problems of acid leakage might be alleviated if suitable neoprene or rubber or plastic bags surround each battery. Not all would be cut after an accident occurs. Also, packages of alkalines or buffers could be provided, to neutralize spills. As for the computer failure, you might be able to get a limp-home mode, when the primary controller/computer poops out.

Then I pointed out to Jim, none of these reasons are enough to cause me to not buy an electric car. Heck, I only commute 44 miles in the morning, and the same at night—not a big deal. But, while the initial cost of the batteries is bad enough, the cost of replacing them every 30,000 miles is significant, since I put on that many miles every 15 months. Many promoters of electric cars ignore or gloss over the costs and problems of finite battery life. They say their operating costs are only 3 or 4 cents per mile, much better than a "typical" gas-powered car at "8 cents per mile." Well, I sure as heck do not pay 8 cents per mile to run my VW to work. Maybe 5 cents per mile, including replacing the engine every 230,000 miles, whether it needs it or not.... If I bought an electric car and it saved me 2 cents per mile, I would have to run it for 20 years to break even, not to mention, get ahead on costs. No, the cost of replacing the batteries periodically, is a significant factor in keeping me from buying an electric car.

Then I commented on the heater problem. You could easily rig a little propane heater, as an add-on accessory. That would keep your feet warm, and your windshield clear for all cold weather. BUT I have done a LOT of driving in Massachusetts. Often, I would drive to work, and the snow would begin, and by the time I wanted to go home, the highways would be 70% clogged with snow, and 80% clogged with stalled cars. You would just KNOW that you could not start out on a trip of 30 miles in conditions like that, in a battery-powered car, and have any serious hope of getting home. So, in some parts of the country, an electric car would just be trouble looking for a time and place to happen.

Then I began to muse about some of the rule-benders that my friends knew, back in Taxachusetts. When you buy a car there, first you pay Sales Tax on it, once, and then you pay "excise tax" on it, annually, forever. If you buy a car with a built-in radio, you pay excise tax on the radio forever, too. So a number of my friends would buy a car with no radio. Then they would buy a good after-market radio, and they would be able to avoid paying excise tax on the radio, forever. Maybe such a person would buy an electric car without a radio—and without a heater. Then after he gets it registered, he could drive down to Lechmere Sales and buy an after-market radio—and an after-market heater. That way he could have a perfectly non-polluting car—but a bolt-on, modular heater. Of course, the car would have to be designed to accept a modular add-on heater, air vents and controls, too. Well, that is a neat solution to that problem. Now, does that suggest anything else?

Well, yes, it does. I think I would like to buy an all-electric, non-polluting, battery-powered car, and then drive down to Lechmere, and buy an add-on, after-market gasoline engine, or maybe a propane engine, or a diesel engine, that I could use to re-charge the batteries. This would be a bolt-on engine-generator set, so any time I wanted to remove it, I could prove that I still had a pure, non-polluting electric car. But when I wanted to go on a long trip, such as to work, I would start down the street, and as I neared

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the freeway, I could start the little engine, and all the way to work, I could keep feeding charge to those batteries. If I got to a traffic slowdown, the batteries would just get better and better charged. As soon as I got to work, I could just leave the engine run a few minutes, and when the batteries got charged up, the engine would shut off automatically.

Hey, now there is a rule-bender! Even better than not having to pay excise tax on your radio, and your heater, and your engine, forever, you could drive a non-polluting car, and charge up the batteries when they needed it, and not discharge the batteries very much. Better yet, you could get along with 1/2 or 1/3 or 1/4 as much batteries as usual. And best of all, the batteries would never get discharged very low because you could keep feeding them charge. So, the batteries get MUCH lighter, and the battery never gets cycled low, so, battery life would be GREATLY increased. And all I have to do is find a modular 5 HP motor-generator.... because I know that a VW can cruise at 55 mph, on the flat, with no headwind, using just about 5 HP. That's about 10 × as much power as the cute little portable motor-generator sets. So, I will have to shop around for a suitable, compact engine-generator set.

Now, while every internal-combustion engine does generate some pollution, an engine designed to run at constant speed and constant load can be designed to run *much* more cleanly than an engine that has to be able to run at light or heavy loads, and at slow or fast speeds. So this car, while not as clean as a car whose batteries are recharged by wind-power or hydro power, can still be a lot cleaner than most gasoline-powered cars. Still, now there is no technical reason I cannot use a "battery-powered" car. Of course, the concept of this "hybrid" car has been around for many years—but, the modular approach seems to bring some new advantages.

Then my brain began to race—maybe I can patent this? I phoned my friend Al, in the Intellectual Property group. I asked him to run a search on this concept—a *modular, removable* engine to go in an electric car. Wow! I could be a hero!! I could be RICH!!!

The next morning, Al showed me a 1993 patent, U.S. patent number 5,225,744, for an electric car with a modular, bolt-in engine, by a couple of Japanese engineers.[1] Well, I had a good idea, but these guys only beat me to it by 3 or 4 years. Sigh. Still, it is a good idea, even if I have to pay royalties to these Japanese guys. They deserve it. So, one of these days, a battery-powered car may indeed be really practical. Even if the snow slows you down, the little engine can keep the battery charged. You would be able to get home—*without* running your batteries down. Worst case, you could stop for coffee, and leave your motor-generator running.

Finally, I threw in one more idea to tickle Jim's fancy. There are some new flywheel modules made by Flywheel Systems, (Seattle, Wash.) that weigh 40 lb, and spin a carbon-fiber rotor up to over 100,000 rpm. When you put 20 of these magnetically-coupled flywheel modules in your car, you'll have enough energy to drive as far as 390 miles. (Estimated, best case.) Admittedly, these flywheels are just in the prototype stage, but they really do have a lot of advantages over batteries. They can be "recharged" many, many times, and you can draw a lot of power out of them without straining their longevity. They are easy to arrange to be modular in parallel, so if one or two quit, you have 19 or 18 to keep you going. Maybe if I combined those with a little 5 HP engine, I would need only 2 or 3 flywheel modules...??? Maybe if I wait just a little longer, I can get all these advantages, without having to design and build the car myself... So, Jim, it sure sounds like fun, in the not-too-distant future.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
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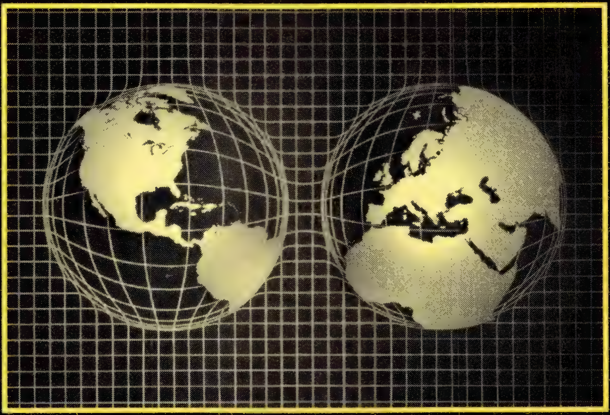
[1] U. S. Patent 5,225,744: Masami Ishikawa and Yukihiro Minezawa; assigned to Aisin Aw Co., Ltd., Japan. Filed April 27, 1991; issued July 6, 1993.

Technology on the Move



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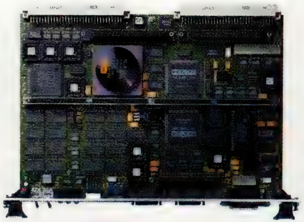

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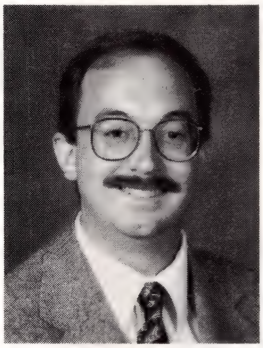
Potentially, personal digital assistants (PDAs) could revolutionize the way people communicate. In fact, they may eventually have the same impact as cellular phones and microcomputers, especially when they're implemented with more useful functions. Within a few years, PDAs will offer the features of a microcomputer, combined with powerful messaging and communicating capabilities. And PCMCIA cards will play a vital role in supplying PDAs with this added functionality. To date, however, PDAs present myriad challenges that makes PCMCIA-compatibility difficult for designers to implement.

Currently, PCMCIA manufacturers are in a holding pattern while the major players within the PDA market fight it out to define the "ideal" PDA architecture. Apple, Microsoft, General Magic, and Geo Works each have developed their own PDA specifications and operating systems. In addition, the specifications were developed from an end-user application viewpoint, meaning that the hardware is defined from a software perspective. Each player employed its own software (operating system) requirements while defining the hardware characteristics, such as the CPU, I/O, memory, and display configuration. Some have even specified a non-standard system operating voltage.



Because the software requirements were the top priority during the PDA designs, there's an abundance of PDA architectures, and some unrealistic approaches. Those companies building the actual PDAs and the accompanying system components, including manufacturers of PCMCIA cards and adapters, are struggling to meet the artificial goals set by the software definers.

In this proliferation of available architectures, no clear winner exists yet. None of the available architectures (or their supporters) has enough clout to build a de facto-standard platform. PCMCIA manufacturers are inundated with an abundance of architectures and no clear direction as to which they should support. What's more, as the demand for PDAs continues to increase, other companies are entering the market. This means that the quest for a standardized PDA architecture is still a long way off.

The PDA operating systems, which are radically different from those employed in mainstream laptop computers, place an additional burden on the PCMCIA manufacturer. The design philosophy has been to develop operating systems that keep pace with the technology of the 90s. For example, object-oriented operating systems are popping up to support the latest wave of PDAs.

Along with structurally different operating systems, new technology must be created for each architecture or PDA device. This means that PCMCIA manufactures working with one system have to start all over again when developing products for another. And there's an extensive learning curve associated with each new operating system. In fact, multiple-platform support is so difficult that PCMCIA manufacturers and developers find it nearly impossible to support more than one platform.

Aside from the differing operating systems, PDAs typically utilize unique memory systems. The traditional file-oriented system found in desktop computers is being replaced by application-oriented systems. Data is being stored in large object-oriented databases, enabling applications to access and share data, even if the data wasn't created by that particular application. This is helpful from the application and end-user points of view, but not for the PCMCIA developer. PCMCIA products are still oriented toward the DOS/desktop-type storage.

Retooling products to meet storage compatibility issues is a definite challenge as PCMCIA manufacturers design products that, for example, interface with larger, integrated databases as opposed to the traditional file structure of DOS-oriented databases.

For a PCMCIA card to work with a laptop computer or PDA, a device driver must be developed for that system. Due to the operating and storage system challenges, there's no straightforward way to develop a PDA device driver or interact with the hardware. Furthermore, the tools necessary to develop PCMCIA cards for PDAs are either inefficient or nonexistent. Add this to the time-to-market issues facing PDA vendors, who are pushed into releasing handheld computing devices as soon as possible, and the environment becomes ripe for relegating peripheral support to the backburner. Thus, PDAs support memory cards, but PCMCIA I/O support (if any) is limited to modems.

For more information on the PCMCIA standard, contact the PCMCIA office at (408) 720-0107.

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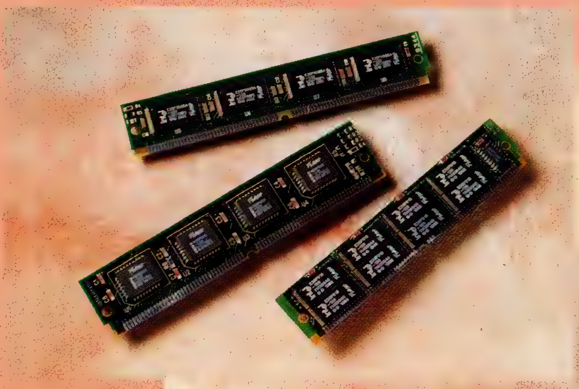

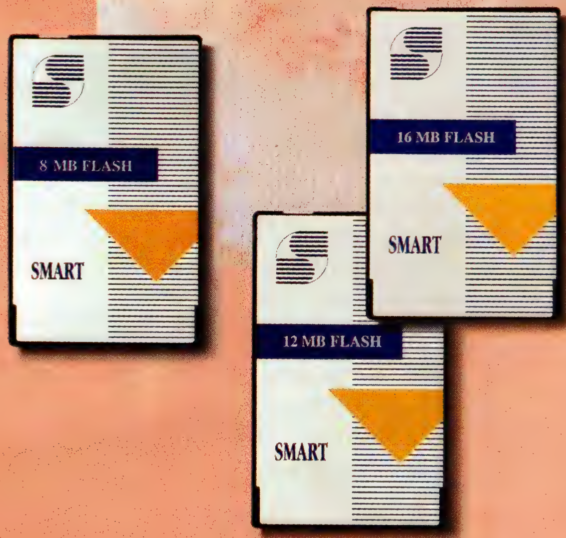

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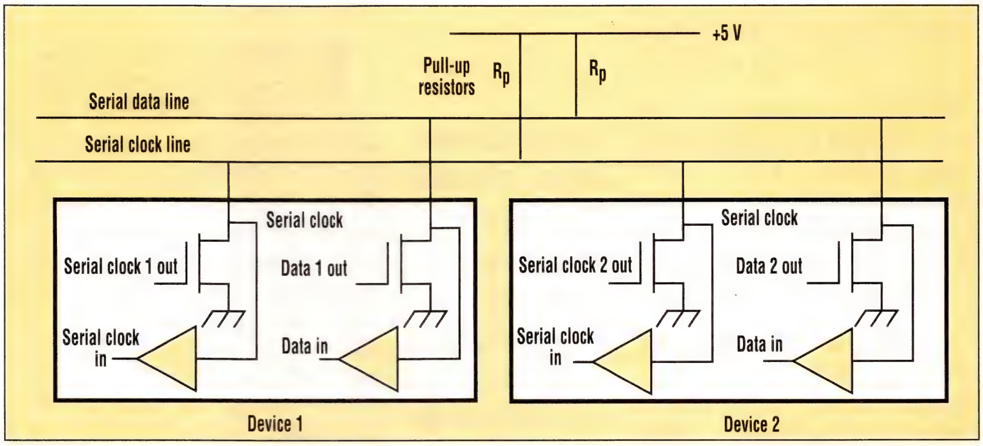
READER SERVICE 110

The ACCESS.bus Offers Improved I/O

Architecture opens the door to PnP for embedded systems.

BY DAVID WYLAND
The Wyland Group, 15213 Bowden Ct., Morgan Hill, CA 95037; (408) 778-3860.
PERETZ TZARNOTZKY
Computer Access Technology Corp, 3375 Scott Blvd., Suite 410, Santa Clara, CA 95054; (408) 727-6600.



1. The I^{2}C bus is a resistor-terminated bus with two wires. One wire is for serial data, and the other is for the serial clock.

The goal of the ACCESS.bus, an avenue for device connectivity, is to simplify serial I/O communications design in embedded systems, potentially replacing RS-232. It includes a hot-plug feature, which means that users can connect or remove devices to and from the bus while the system is running. This is an advantage in real-time systems that must remain on line continuously.

Another feature is its universal serial communication over one cable between the CPU and such I/O devices as a keyboard, mouse, and other peripherals that work with the PC. The asynchronous serial bus, which is an open industry standard, is similar to RS-232 communication with some additional features and without some of the baggage that RS-232 carries. The standard comes from a collaboration between Philips and DEC.

The ACCESS.bus is a two-signal, four-wire communications interface that connects the CPU to the peripheral devices through a modified four-wire modular telephone plug. Two of the wires are for a serial clock and data, one is for ground, and the last supplies +5 V for the I/O peripherals.

All devices on the ACCESS.bus are connected in parallel in the same way that extension telephones are connected. Up to 125 devices can be connected to one bus, as limited by the addressing scheme and by capacitive loading. The bus transfers multibyte messages one byte at a time at rates up to 100 kbaud. It's similar to RS-232 except that there's one start and one stop condition for each multibyte message rather than for each byte. The sender and receiver automatically adjust their baud rates to the slower of the two. No baud-rate or other settings are needed.

The host CPU assigns each ACCESS.bus device a unique 8-bit soft address at power-up or whenever a new device is connected to the bus. Soft addresses mean that address jumpers and conflicts are eliminated.

The ACCESS.bus supports the coming Plug-and-Play (PnP) standard. PnP devices can be added to the ACCESS.bus system at any time. To make this happen, however, the operating system must recognize the PnP device and then activate the device's software drivers. The system's software handles all installation and activation transparently. The ACCESS.bus uses the soft addressing to implement PnP. Address-assignment software identifies the device, assigns the device a soft address, and then activates the appropriate driver.

Basically, the ACCESS.bus is a software layer that sits on top of existing hardware. The Inter Integrated Circuit (I^{2}C) bus is used as its physical layer. Philips has employed the I^{2}C bus for years as a communications bus between ICs in TVs and other consumer products (in fact, over 150 different ICs employ this interface, including various 8051-type microcontrollers).

The resistor-terminated I^{2}C bus has two main wires (there also is a third wire for ground)—one for the serial clock and the other for serial data that employs TTL-compatible signal levels *(Fig. 1)*.

A sending device drives the clock and data lines with pull-down drivers. The serial clock line's rising edge sends the serial data into the receiving device. This is where the automatic baud-rate control comes into play: The sending device can transmit data as fast as it wants, but if the receiving device isn't ready for the next bit, it holds down the serial clock line until it's ready. Data isn't clocked into the receiving device (or out of the sending device) until the clock's rising edge, resulting in a transparent, automatic baud-rate control mechanism (clock synchronization).

The ACCESS.bus adds a fourth wire to the I^2C bus—+5-V power. Up to 1 A is available at +5 V for devices attached to the bus. This allows for the connection of low-power devices, such as sensors and relay drivers, without requiring a separate power supply.

Multibyte messages are sent by the ACCESS.bus one byte at a time, similar to RS-232 asynchronous serial communication. In the ACCESS.bus protocol, all data is written (sent from a sending device to a receiving device).

ACCESS.bus messages are a minimum of five bytes long. Message transfer begins with a unique start condition—a high-to-low transition of the data line while the clock line is high *(Fig. 2)*. This is a special condition because the data line isn't supposed to change while the clock is high except for start and stop conditions. Each data byte is sent starting with the most significant bit and ending with an acknowledge bit from the receiving device. Unlike RS-232, the receiver acknowledges each byte. The message ends with a stop condition, which is a low-to-high transition on the data line while the clock is in the high state.

Transmission-error monitoring is used by the ACCESS.bus to implement CDSMA (collision detection sense, multiple access) bus arbitration, similar to Ethernet. If two sending devices attempt to control the bus simultaneously, data from those devices will interfere when one device tries to drive the bus high while the other drives it low. This doesn't create a hardware problem; the data is merely wire-ANDed by the bus' resistor-termination architecture. However, the device unsuccessfully attempting to drive the bus high will discover the interference, get off the bus, and wait for the bus to be idle before trying again. The other device detects no error and continues. Transmission-error monitoring also eliminates transients caused by hot plugging when a transmission is in progress. The sending device will detect this error and retransmit the message, if necessary.

Its own device-driver software eliminates software and hardware installation, making ACCESS.bus truly plug-and-play.

The I^2C bus protocol defines the rules for sending multibyte messages, while the ACCESS.bus protocol defines the rules for sending its message blocks (the basic transfer mechanism of the ACCESS.bus). Each message contains a 3-byte header, a 1- to 127-byte command or data block, and a checksum. The header consists of a 1-byte destination address, a 1-byte source address, and a data-block length. The source and destination addresses contain 7 bits. The least significant bit of each address byte is always zero. The ACCESS.bus protocol reserves three of the 128 possible addresses (00h, 50h and 6Eh), allowing soft-address assignment of up to 125 devices on the bus.

When assigning soft addresses, rather than set unique address jumpers for each device (with the possibility of getting them wrong), the CPU assigns the addresses at power-up and whenever a new device is plugged in. The address then is written into the device's address register. There's nothing sacred about addresses; the CPU just uses them to differentiate between devices. As long as the CPU knows which address belongs to which device, everything operates correctly.

When the system powers up, all devices listen to the default address (6Eh). The CPU then sends a broadcast reset signal to every device on the ACCESS.bus. Following this command, all devices send an Attention message, requesting a new address. The CPU responds with an Identification Request, which is followed by an Identification Reply from each device. The CDSMA protocol makes it possible for the CPU to read one message at a time. The Identification Reply message contains a 29-byte identification string with a unique 32-bit serial number that lets the CPU distinguish between identical devices. The CPU records this data, picks the next available address, and sends it to the subsequent device with a copy of the 29-byte identifier as part of the Assign Address message. Each device compares the ID string to its own ID string until there's a match, and at that time is assigned a soft address. This process continues until there are no more devices sending Attention or Identification Reply messages.

The 29-byte identifier string received from the device typically includes information about the device, such as the manufacturer, model number, and revision level. In addition, the CPU can send a Capability Request message to the device with its new address, which is followed by a Capability Reply message that can be up to 64 kbytes long. Using the Capability Reply, the device supplies its own device-driver software. This eliminates software and hardware installation, making the device truly plug-and-play.

Although the CPU assigns the addresses, most communications come from applications software, the operating system, or software device drivers. The ACCESS.bus Manager software driver connects the ACCESS.bus devices to their corresponding operating-system drivers. This connection is initiated by the device driver.

A device driver that needs the services of a specific peripheral calls the ACCESS.bus manager and asks to be connected through a Link Request with that device. The Manager searches the device table for the requested device and then sends

IF IT SHAKES RATTLES OR ROLLS OR SPINS RECORDS PUSHES PULLS COMPRESSES TRANSFERS MEASURES PLACES SHIFTS PRINTS DROPS GRINDS SWAPS PLAYS LIFTS SPLITS BAKES CUTS ETC. ETC. ETC.

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a Link Reply. The driver approves the connection by sending a Link Approval. If the Manager can't find a matching device, it records the request and waits for the required device to be connected. Upon connection, the Manager automatically offers the device to the driver that requested it.

One of the most common communication methods used in computers, including embedded systems, is RS-232-based asynchronous serial I/O. It's relatively simple, inexpensive, and widely available. It's extensive usage is partly due to the fact that it was the first communication standard for computers, based on the original 110-baud mechanical teletype devices.

One problem associated with RS-232 communications, though, is that one cable is needed for each device. Various non-standard RS-232 derivatives are available that reduce the UART hardware and cabling. However, the RS-232 connector and signal-level standards define one port talking to one device.

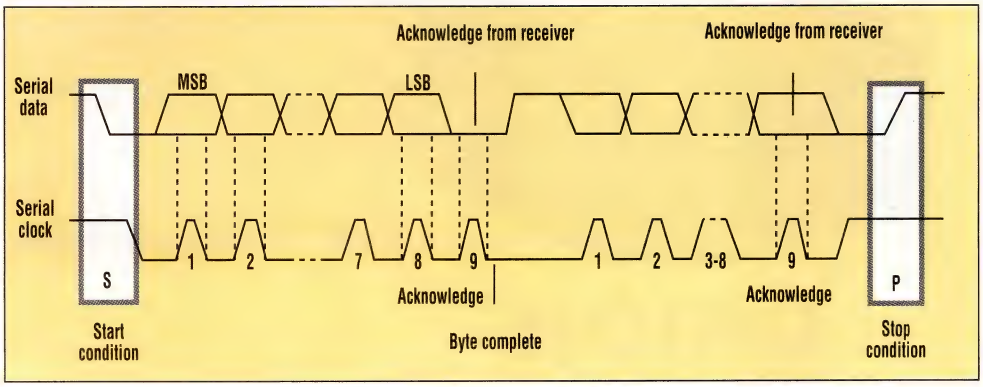
Another problem involves the many off-shoots of the RS-232 standard. For example, the cable could have a 9- or a 25-pin male or female connector. Other questions concerning the internal hardware configuration that must be answered include: What is the baud rate, the number of bits per byte, the parity type, and the number of stop bits in the string? If the RS-232 I/O port and its associated I/O device don't have the same configuration, the hardware won't operate properly.

Finally, designers must consider the RS-232 signal levels, which are about +12 to –12 V for a logic high and low, respectively. To attain these levels, special ICs and power-supply considerations are needed for most systems. In many PCs, +12 V is used only by the disk drives, and –12 V isn't even available. In most portables, not even +12 V is available. Also, these high-voltage ICs are usually the first to burn out if there's an RS-232 cable problem. These issues can affect the cost and reliability of the RS-232 devices.

The good news is that the ACCESS.bus supplies RS-232-style communications while eliminating the problems associated with RS-232. Because of its bus architecture, only one ACCESS.bus port is needed on the CPU. And only one cable is required to daisy-chain through all of the ACCESS.bus devices in the system, rather than the one port and cable per device needed for RS-232. The ACCESS.bus' small cable and connector is less expensive and easier to work with than the bulky 25-wire cable and connector used by RS-232. In addition, the ACCESS.bus connector comes in only one style, further reducing incompatibilities.

Internal hardware-configuration problems are avoided because there are no baud-rate, bits-per-byte, parity, or stop bits to set. Because the ACCESS.bus uses a +5-V resistor pull-up bus, no special power supplies are required.

2. Message transfers begin with a high-to-low data transition while the clock line is high. The message ends with a low-to-high transition on the data line when the clock line is high.



The ACCESS.bus combines solutions to some long-standing RS-232 problems with additional features that are particularly valuable for embedded systems. Up to 125 devices can be connected to one I/O port, requiring just one IRQ line and CPU I/O address. The hardware autoconfiguration and soft addressing is valuable to the embedded-system designer because it reduces the time and trouble required to get a device up and running. In addition, the ACCESS.bus' high speed helps to reduce system latency and response times.

Computer Access Technology Corp. (CATC), Santa Clara, Calif., and Philips Semiconductors, Sunnyvale, Calif., have announced support for putting the ACCESS.bus on a PC motherboard. The companies supply an 8xC542 microcontroller with CATC microcode to replace the standard 8042 keyboard controller used on PC motherboards. The upgraded motherboard runs both standard keyboards and ACCESS.bus devices.

The ACCESS.bus has no license fees or royalties. It's supported by the ACCESS.bus Industry Group (ABIG), Sunnyvale, Calif., which is a source for technical data and vendors (the ABIG can be reached at (408) 991-3517).

David Wyland is the president of the Wyland Group consulting organization.

Peretz Tzarnotzky, a founder and the vice-president of engineering at Computer Access Technology Corp., graduated from the Technion Institute of Technology in Israel.

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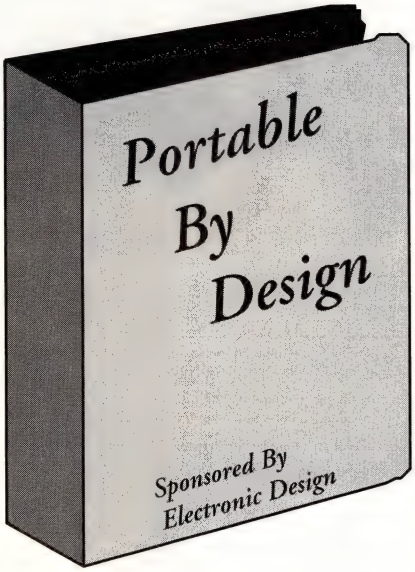

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SYSTEM DESIGN NEWS

To speed the development of multimedia support circuits, designers at Western Digital's Imaging Products Div., Mountain View., Calif., inked a licensing agreement for MPEG video compression/decompression technology from Mediamatics Inc., Santa Clara, Calif. The MPEG technology, dubbed collaborative compression architecture (CCA) by Mediamatics, will be embedded into a forthcoming family of graphics chips that include algorithm acceleration to deliver 30-frame/s motion video at lower costs than are now possible. The CCA approach allows the algorithms to be partitioned between the CPU (software execution) and dedicated silicon (hardware acceleration) to best fit cost and performance needs. Contact Western Digital's Sam Sanchez at (415) 335-2581 or Mediamatics' Prem Nath at (408) 496-6360.

Adding a display data channel (DDC) to video monitors and using the serial ACCESS.bus as the control bus to link the monitor to the host system recently was given unanimous approval by members of the Video Equipment Standards Association, San Jose, Calif. With the DDC, computer monitors can achieve full "plug and play" capability: When plugged in, the monitors will be able to automatically notify the host computer upon power-up of their specific capabilities and configuration. Furthermore, users can control the monitor features (vertical/horizontal position, brightness, contrast, etc.) by setting up a software control panel and sending control information over the DDC to the monitor. Monitors incorporating the DDC are expected to be released by various suppliers starting later this year. Contact the ACCESS.bus Industry Group at (408) 991-3517.

With an aspect ratio of 16:9 and a resolution of 1920 by 1080 pixels, a soon-to-be-available monitor is able to deliver a movie-screen-like display area, ideal for CAD, desktop publishing, and other applications that require large-area displays. Using the HDTV format, designers at Sony Electronics, San Diego, Calif., employ their Trinitron technology to build a 30-in. color display tube that delivers a useful screen area of 620 by 372 mm (24.4 by 14.6 in.) with scan rates of 60 or 72 Hz vertical and 70 or 84 kHz horizontal. The high-resolution GWM-3000 delivers photographic quality and allows 0.1-in.-high characters to be read anywhere on the display surface, with convergence levels to within 0.3 mm in the central region of the screen and within 0.4 mm on the outer edges. The monitor requires video-card drivers that deliver noninterlaced dual-scan signals with a dot clock of 216 MHz at a 72-Hz refresh rate (180 MHz with a 60-Hz rate). A few such cards exist for PCs, and Sony expects more higher-speed cards to be offered in the near future. The high resolution, though, won't come cheap—the preliminary price in single quantities is about $33,000. Contact John Wyckoff III at (619) 673-2860.

A small-footprint digitizing tablet that's just 6 by 8 in. and less than 0.5 in. thick delivers a resolution of 2540 points/in. with an accuracy to within 0.010 in. Developed by Kurta Corp., Phoenix, Ariz., the tablet provides the 6-by-8-in. active area in an 8.5-by-11-in. frame, occupying no more desk space than a standard note pad. For data entry, the tablet uses a four-button cordless cursor, a non-pressure-sensitive pen for signature capture or handwriting recognition, or a pressure pen for drawing that provides up to 256 levels of pressure and the natural feel and control of a fine drawing instrument. Along with the 6-by-8-in. XGT tablet comes the VisualTablet software developed by Multipoint, which provides pop-up on-screen menus and customizable templates. The software allows screen and active area scaling, permitting users to modify the size without leaving the application. The tablet includes a serial interface to a host computer and comes bundled with the cursor, VisualTablet software, and both DOS and Microsoft Wintab drivers for $395. An optional battery pack is available to let the tablet operate virtually anywhere. Contact Kurta at (602) 276-5533.

▼ LOW-COST GRAPHICS BOARD RUNS AT 64 BITS

Operating in the DOS-Windows environment, the WindowsVGA 64 is a video-graphics accelerator that can handle 64-bit data. The board supports true color (16.7 million colors) at a resolution of 1024 by 768 pixels. Its maximum resolution is 1280 by 1024 pixels. Based on the Cirrus Logic CL-GD5434 graphical-user-interface chip, the board employs a 64-bit memory interface and is available in either a VL-Bus or PCI configuration. Advanced drivers are included for most popular software environments and applications, including Windows, Windows NT, OS/2, AutoCAD, AutoShade, 3D-Studio, Lotus 1-2-3, and WordPerfect. Software-driver updates can be downloaded from the company's bulletin board. The WindowsVGA 64 board comes in two versions, both employing DRAM. The 1-Mbyte model can be upgraded to 2 Mbytes and the 2-Mbyte base unit can handle 4 Mbytes. Prices start at $199, with large-quantity discounts available.

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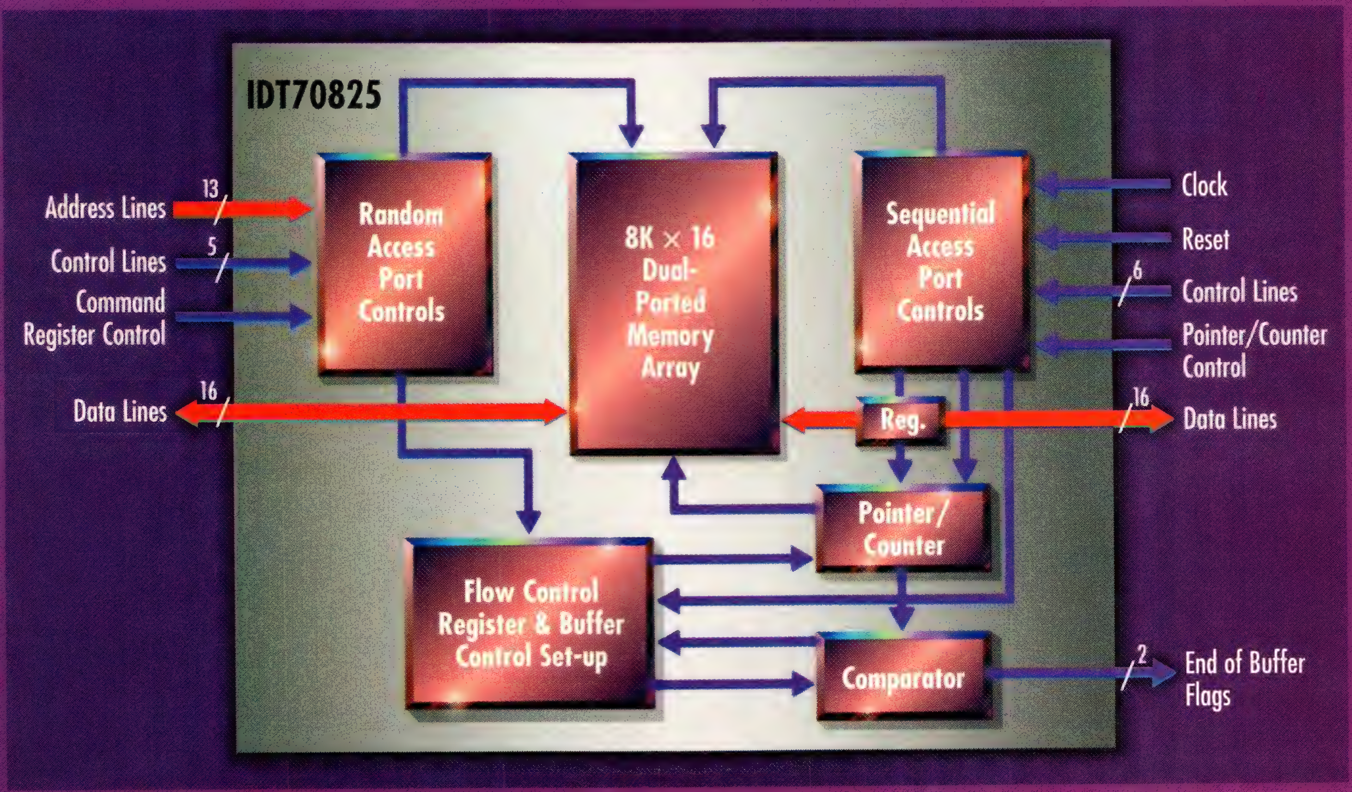

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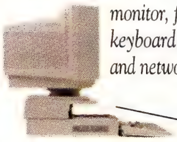

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▼ DISK CONTROLLER CONNECTS TO PCI BUS

As PCI-based systems begin to emerge, users of such systems are on the lookout for compatible peripherals. The DAC960P is a RAID controller board that plugs into the PCI bus and can handle internal or external disk arrays. It supplies increased performance and fault tolerance for networks and workstations running such applications as full-motion video and graphics. The board offers a sustained sequential read throughput of up to 30 Mbytes/s. Available in one-, two-, and three-channel configurations, the RAID controller is built with an i960CF 32-bit RISC microprocessor and an onboard cache that employs from 2 to 32 Mbytes of standard DRAM or faster EDRAM SIMMs. The DAC960P supports NetWare, UnixWare, Windows NT, OS/2, Banyan Vines, SCO Unix, and other PC-based operating systems.

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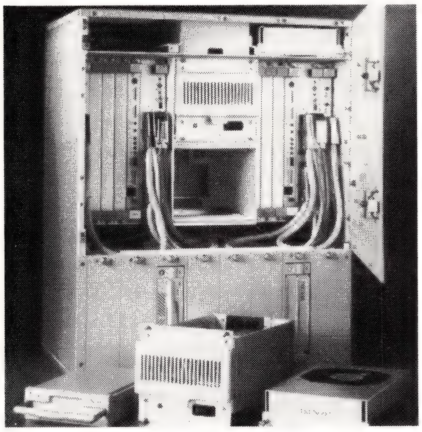
▶ CIRCLE 603

▼ SPARC SERVER BOASTS FAULT TOLERANCE

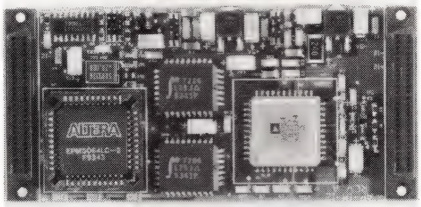
The Gemini fault-tolerant communications server offers a fully-redundant high-performance Sparc processor in a rugged enclosure. The Gemini, with its dual Sparc processors, is aimed at industrial applications such as supervisory control and remote data acquisition and control. Measuring 26 by 17.22 by 10 in., the system is available in either a 19-in. RETMA or 24-in. telecom rack enclosure. The replicated system duplicates all components in one enclosure. The software environment is layered on top of Solaris, which replicates application software on two or more processors. Other features include SCSI 2 and Ethernet controllers, a shared-disk storage subsystem, and disk mirroring. At least two SBus and seven VMEbus slots are available, as well as bays for up to eight 3.5-in. half-height peripherals. Available now, the Gemini fault-tolerant system starts at $50,000.



Themis Computer Inc.
6681 Owens Dr.
Pleasanton, CA 94588
(510) 734-0870
▶ CIRCLE 604

▼ MODULE OFFERS 12-BIT A-D CONVERSION

Designed to meet a single-width IndustryPack form factor, the IPS-ADC10 is a 12-bit analog-to-digital converter that operates at programmable sample rates from 150 kHz to 10 MHz. The module features FIFO buffering for up to 32,000 samples, supports DMA transfers, and includes on-board control and status registers with support for interrupts, which can be clocked and triggered internally or externally. Multiple modules can be combined for simultaneous sampling. An integral linearity of ±2.5 LSB can be achieved, with a differential nonlinearity of ±0.5 LSB. The signal-to-noise distortion is 65 dB and the total harmonic distortion is –70 dB at an input frequency of 1 MHz. Up to four modules fit onto the CommIO carrier card, which employs four 20-Mbyte/s TMS320C40 communication ports to route data in a point-to-point manner between the IndustryPack modules and other VMEbus DSP cards. The IPS-ADC10 sells for $2495.



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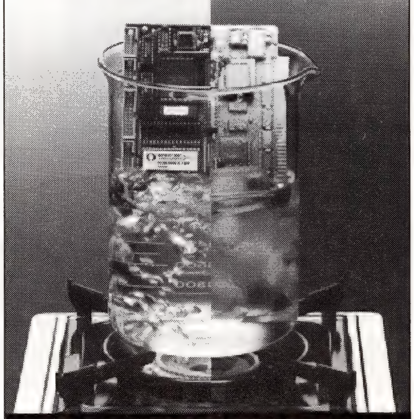

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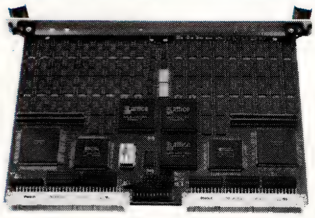

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SYSTEM DESIGN PRODUCTS

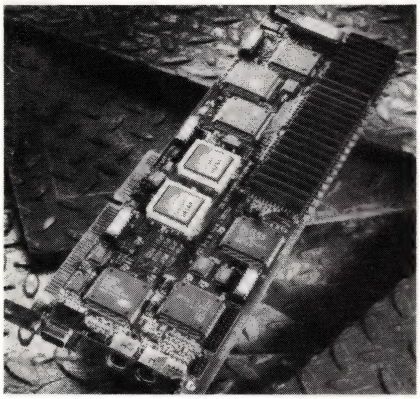
▼ DSP MODULE FEATURES HIGH-QUALITY AUDIO

The M4-0202-A standalone, digital-audio, signal-processing module reduces the time needed to develop high-quality, digital-audio products. The application board, designed for embedded audio processing, is targeted at prototyping and small-scale production. The module is based on a Motorola 56004 digital-signal processor and uses 18-bit analog-to-digital and digital-to-analog converters. Other features include an overall dynamic range of 100 dB, on-board bootstrapping for nonvolatile SRAM or EEPROM, and an expansion connector for user interfaces. The M4-0202-A module sells for $695. An evaluation pack is available that includes the module, a manual, software (I/O routines, sample applications, and examples), and information on the 56004 DSP. It costs $1995. Development tools also are available.

Sample Rate Systems Oy
Kanslerinkatu 14
FIN-33720 Tampere, Finland
+358 31 3165 045
▶ CIRCLE 606

▼ VIEW TWO VIDEO INPUTS ON A DISPLAY

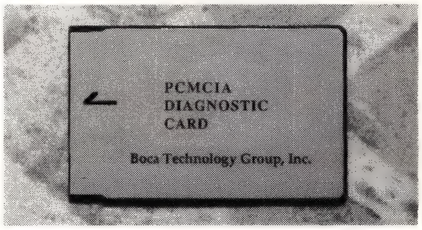
Users can now view two separate full-motion video inputs, one live and one compressed, and display four different moving images simultaneously on a desktop PC. This capability is enabled by the MegaMotion board, which supplies the ability to capture images at 30 frames/s with a resolution of 320 by 240 pixels. JPEG video compression helps to improve disk utilization for image storage. The board offers a complete array of editing special effects, such as Alpha channel, fades, mixes, and wipes, and advanced frame capture for complex graphics. In addition, MegaMotion supports Gamma correction, video cropping, and full-color bars in video input and output modes. Available now, the board sells for $1095. It comes with 1 Mbyte of VRAM and a 2-Mbyte frame buffer to store video images, eliminating the need for a separate graphics accelerator card. MegaMotion is bundled with Adobe's Premier to provide video-editing features.



ASL Inc.
2361 McGaw Ave.
Irvine, CA 92714
(714) 252-0117
▶ CIRCLE 607

▼ DIAGNOSTIC CARD HELPS DEBUG PCMCIA SLOTS

Development, manufacturing, and systems engineers designing devices with PCMCIA card slots often have difficulty ensuring that the interface is completely compatible and functional. Expensive in-circuit testing equipment isn't always feasible.



The BGM64 PCMCIA diagnostic card helps solve that problem at both 5 and 12 V. The card plugs into the slot, allowing the designer to wrap the data and address buses through the PCMCIA interface. PCMCIA host software helps test all 16 data bits on an emulated 64-Mbyte address space. Both reads and writes are possible. A register interface on the card can help emulate low-battery conditions by driving the BVD1 and BVD2 signals high or low. Card detects, write protect, wait, and reset signals also can be tested. The BGM64 diagnostic card sells for $249. A 365SL-compatible developer's kit with host software and source code that's being readied will go for $4500.

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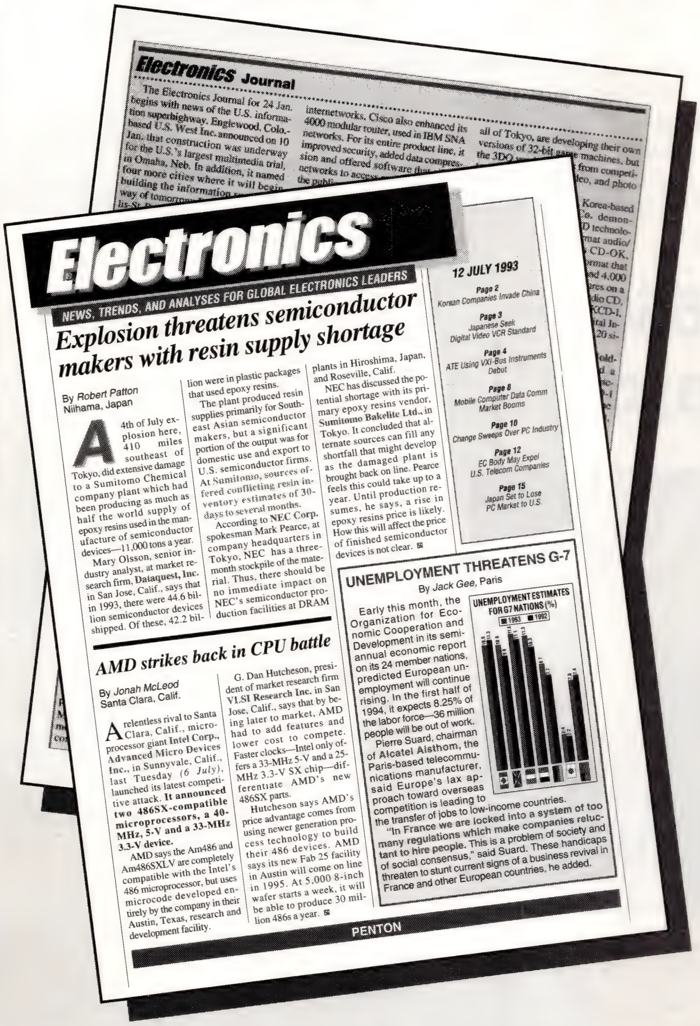

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

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Japan Set to Lose PC Market to U.S.

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ■

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ■

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of **Alcatel Alsthom**, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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▼ SOUND BOARD HOLDS YAMAHA WAVE-TABLE CHIP

The Yamaha OPL4 wave-table sound chip is the centerpiece of the Golden Sound Pro 16 Plus sound card that offers professional-quality audio. The board features true 16-bit record and playback, a built-in SCSI-2 CD-ROM interface, stereo microphone adapters, and an integrated Adaptec AIC-6360 SCSI interface chip. It's compatible with most popular audio standards, including Windows Sound Systems, Sound Blaster, and General MIDI. The board can pass data at 10 Mbytes/s. The Golden Sound Pro 16 Plus sells for $299. For stereo surround and echo effects, an optional daughterboard can be plugged in.

Toptek Technology Inc.
14140 Live Oak Ave., Unit C
Baldwin Park, CA 91706
(800) 874-4425
or (708) 291-1616
▶ CIRCLE 609

▼ VL-BUS EXTENDER ALLOWS HOT SWAPPING

To expedite the testing and development process of VL-Bus products, the VESA Local Bus Electronic Extender (VEE) lets users insert and remove adapter cards (hot swap) from a PC without powering down the system. This feature saves time during testing and reduces wear on the PC by eliminating the rebooting process. The VEE offers adjustable overcurrent sensing circuitry, which senses excessive current consumption and protects the PC power lines by automatically disconnecting the tested card if an overcurrent condition is detected. The power and bus signals of the card under test can be controlled using a hardware switch or with software controls to supply completely automated testing. The VEE (part #9900-12-10) costs $749. Large-quantity discounts apply.

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▼ SCSI 2 ADAPTER FITS PC/104 FORM FACTOR

System designers now can implement an SCSI-2 interface using a PC/104 module. The SCSI-104 is compatible with the Adaptec AHA 1520 SCSI-2 interface and supports 10-Mbyte/s fast-SCSI operation. The module also includes two serial ports and a PC/AT floppy-disk drive controller. The SCSI-104 comes with onboard BIOS, an Adaptec software driver, and the Adaptec EZ-SCSI configuration utility. The BIOS lets the SCSI hard disk boot using either DOS or Unix. The module is built with a 16-bit ISA interface and an 8-bit single-ended SCSI interface. In single quantities, the SCSI-104 sells for $225.

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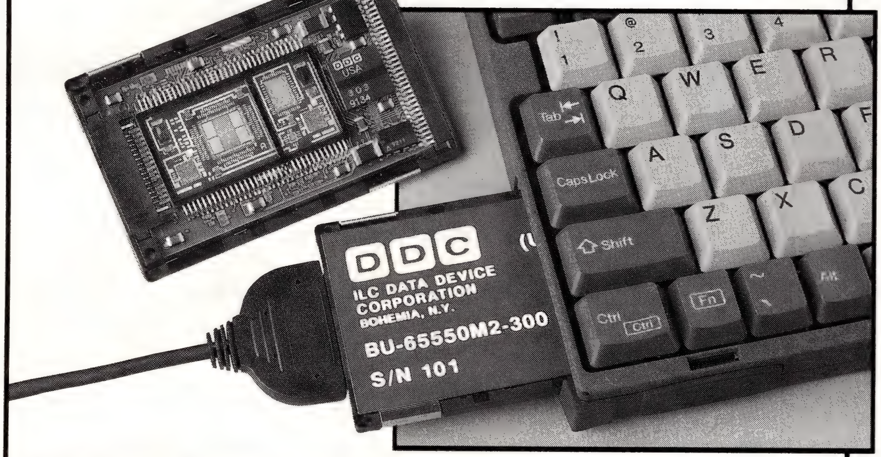
The first MIL-STD-1553 PCMCIA Card



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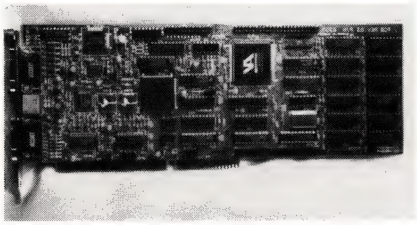
▼ LOW-COST BOARD OFFERS REAL-TIME AUDIO, VIDEO

Audio and video can be captured and played back on the VideoPacker Plus board. The low-cost board, which is based on Auravision's VxP50 chip, combines high-quality motion video and 16-bit audio with VGA-generated graphics. What results is full-screen motion video that uses a real-time hardware interpolation zoom capability.



The board digitizes, displays, stores, and plays back NTSC, PAL, or S-Video from a television or VCR in real time. The VideoPacker Plus also is compatible with camcorders, CCD cameras, laser-disk players, and optical drives. Available now, the board sells for $375. That price includes the card, image-editing software, and drivers for Windows 3.1 and Video for Windows.

VIC Hi-Tech Corp.
2221 Rosecrans Ave.
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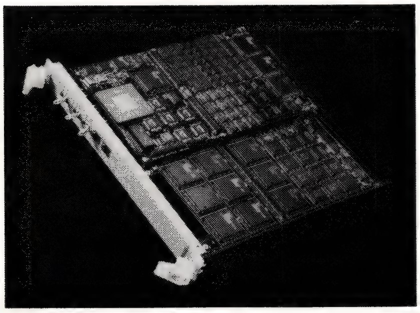
(310) 643-5193
▶CIRCLE 612

▼ 64-BIT RISC CPU DRIVES FUTUREBUS+ SBC

The 64-bit Mips R4600 RISC microprocessor is the core around which the NR4600-1 Futurebus+ processor board is built. Applicable systems range from diskless single-board computers to multiprocessor systems. To supply a high degree of interoperability with other Futurebus+ modules in an integrated platform, the board is designed with all of the required features listed in Profile F of the IEEE 896.2 Futurebus+ specification. The NR4600-1 features a single-transaction write buffer, 4 Gbytes of physical address space, up to 2 Mbytes of flash memory, and up to 32 Mbytes of DRAM. Half of the DRAM is accessible from both the bus and the 100-MHz CPU, while the other 16 Mbytes is only accessible to the processor. A mezzanine slot is available to customize the board using daughterboard modules. With 2 Mbytes of DRAM, the NR4600-1 sells for $7995.



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READER SERVICE 112

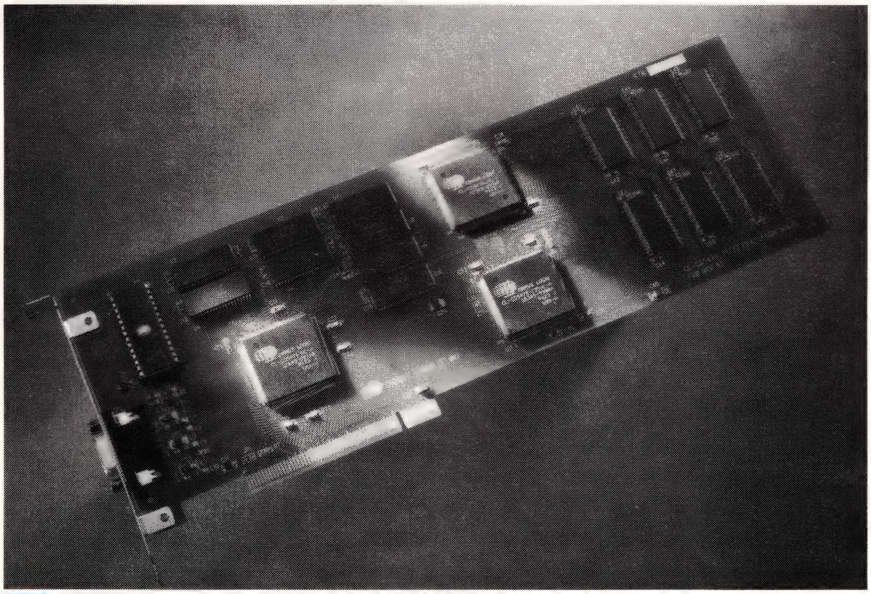
CHIP SET PUTS 3D HIGH-END GRAPHICS ON A PC

BOARD DEVELOPERS CAN BUILD WORKSTATION-CLASS 3D ACCELERATORS AT PC PRICES.

RICHARD NASS

The ability to display three-dimensional graphics is essential for such applications as CAD, medical imaging, chemical modeling, and animation. The biggest obstacle posed by 3D functionality, however, lies in the cost of a 3D-capable system. Workstations that deliver 3D graphics typically start at about $20,000.

That tune may change, though, with the three-chip set released by Cirrus Logic Inc. The company's Mondello chip set, which consists of the CL-GD5470, 5471, and 5472, gives designers a video-based solution that can run under Microsoft Windows 3.1 on a PC *(Fig. 1)*. The chip set handles the three main operations required for 3D graphics: geometry, lighting, and rendering. A hardware-acceleration capability expedites the development of 3D software applications on the PC. Without such acceleration, 3D software is rendered virtually useless. In addition, the chip set features a standard applications programming interface (API) and supports a wide range of graphics libraries for three dimensional PC-based graphics applications.



1. THE THREE-CHIP MONDELLO CHIP SET created by Cirrus Logic offers workstation-quality 3D graphics at PC prices. Boards built with the chip set can connect to either the PCI or VL-Bus local bus to ensure high-performance operation.

The latest wave of high-performance microprocessors, such as the Pentium and the PowerPC, offer the required processing power for the mathematically intensive geometry and lighting portions of the 3D graphics. The algorithms are mathematically intensive operations which are suited for execution on the host CPU. But the rendering portion requires specialized hardware, which is where the Mondello chip set steps in.

ACCELERATOR IC

In 3D graphics, geometry and transformation operations are needed to compute the vertex positions of polygons that represent 3D objects. New vertex positions must be recalculated in real time as the user manipulates the 3D objects. Once the new positions are determined, the effect on the color of the vertex positions is computed, which is otherwise known as the lighting operation. This color depends on the type of light source, the angle of incidence, the surface characteristics, and the viewing angle.

Rendering involves the actual computation of the pixel values to be written into the frame buffer. The geometry and lighting engines feed vertex data to the rendering engine. In such an engine, each pixel consists of X, Y, and Z positions and RGB color data. The rendering engine interpolates pixel positions and colors and writes these into the frame buffer for screen display.

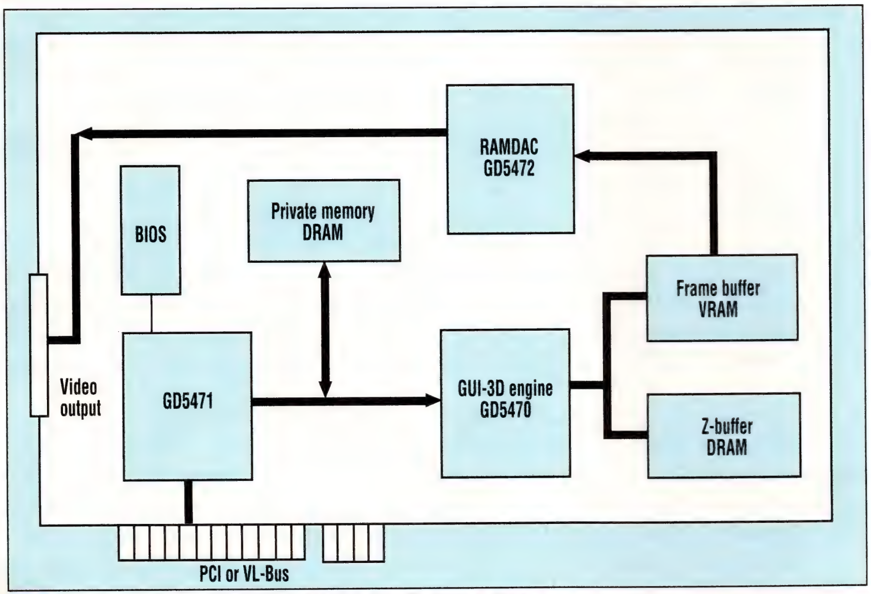
RENDERING PIXELS

The GD5470 3D and graphical-user-interface (GUI) accelerator executes the rendering portion of the 3D graphics pipeline while also handling 2D GUI acceleration (for Windows acceleration). Hardware support is included for both 2D and 3D graphics operations, including vectors, polygons, Gouraud shading, antialiasing, Z buffering, alpha blending, and various BitBLT operations. A high-level instruction set lets the device operate as a processor, a coprocessor, or both.

The chip can draw 1.3 million 2D vectors/s and 250,000 independent 3D-shaded, alpha-blended, Z-buffered polygons/s. It's also capable of 66 Mpixels/s using source-destination block transfers and 22 Mpixels/s using complex source-destination transfers with Z compare. Some integrated features improve image quality as well, such as sub-pixel positioning, which is combined with alpha blending to perform antialiasing of lines, images, and fonts. The 5470, like all three parts in the Mondello chip set, resides in a 208-pin quad flat pack (QFP). All are fabricated using a 0.8-µm CMOS technology.

An interface chip, the GD5471, connects the rendering chip to the system local bus, which can be either the PCI or VL-Bus. The chip also supplies a glueless interface to the Super VGA output. On the PCI bus, it offers burst support of up to 33 MHz, and up to 50 MHz on the VL-Bus.

The third chip, the GD5472, is a 135-MHz dedicated 24-bit palette digital-to-analog converter (DAC) that features a 96-bit-wide direct video RAM (VRAM) interface and a 32-bit video-overlay port with color-key support. The chip supports on-the-fly color-depth changes, allowing 3D animation to employ double buffering. When the animation sequence stops, the resolution changes to 24-bit true color. This allows near true-color, double-buffered animation with 1024-by-768-pixel resolution in a 3-Mbyte frame buffer. Other supported resolutions include 640 by 480 pixels, 800 by 600 pixels, and 1280 by 1024 pixels.



2. TO BUILD A 3D-CAPABLE BOARD, all that's needed is the Mondello chip set, three banks of memory (private memory, a frame buffer, and a Z buffer), and BIOS. Cirrus Logic says that boards should appear with end-user prices falling in the $500 to $600 range, depending on the memory configuration.

A LOW-COST SOLUTION

By using the chip set, OEMs can design graphics boards that retail for about $500 to $600, depending on the amount of memory used. Basically, all that's needed to build a complete board is the chip set, memory, and BIOS *(Fig. 2)*. A low-end board would typically take 1 Mbyte of private DRAM for font caching, 1 Mbyte of VRAM for the frame buffer, and a 2-Mbyte DRAM Z buffer. A higher-performance model would require 2 Mbytes of private memory and 3 Mbytes of VRAM, as well as the 2-Mbyte Z buffer.

The chip set's compatibility with existing graphics libraries should increase the demand for 3D graphics capability on the PC. It's also compatible with current and next-generation Windows operating systems and Solaris, Version 2.4. As a result, software developers can build applications that work with Silicon Graphics' OpenGL and Intel's 3DR graphics libraries, as well as game APIs such as RenderMorphics' Reality Labs, Ithaca's Hoops, and VESA's VAGI. Cirrus Logic is currently working with developers on various applications, including CAD, virtual reality, and games. The company is also a licensee of Argonaut's BRender game API and will offer support for this library under DOS and Windows 3.1 and 4.0.

Microsoft recently licensed the OpenGL graphics library and will include it in the next release of Windows NT and Windows 4.0. This should enable the broad base of OpenGL applications to migrate to the PC. The existing software will have to be recompiled to run on a Pentium or PowerPC microprocessor. ☐

PRICE AND AVAILABILITY

The Mondello chip set is sampling now for $150. Production will commence in the fourth quarter. In 1000-piece quantities, the set will sell for $100.

Cirrus Logic Inc., 3100 West Warren Ave., Fremont, CA 94538; (510) 623-8300.

CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

PRODUCTS NEWSLETTER

BAREBONE SYSTEMS HOLD PENTIUM CPUS

A series of bare-bone systems from Lion Computers, Milpitas, Calif., are based on 486 and Pentium microprocessors. They also are based on the company's NiCE motherboards, which incorporate PCI, ISA, VL-Bus, and EISA buses in different configurations. Each system includes a power supply and case, a 101-key keyboard, and hard- and floppy-disk-drive controllers. High-resolution, 14- and 15-in. monitors are available. An internal CD-ROM drive and sound card can be bundled for multimedia applications. The systems include 256 kbytes of cache memory and starts at $230. Call (408) 943-1100. *RN* **CIRCLE 661**

SOFTWARE SPEEDS GRAPHICS FILES

Fast retrieval and repaint speeds using unique redraw algorithms highlight the Retreeve Express family of Windows-based engineering-management systems from Micro Design International, Orlando, Fla. Features include display of all Intergraph 2D and 3D CAD vector files, with full support for reference file-level display; multiple windows for the same file containing different views or orientations; display of raster file formats including TIFF, CAL, CIT, PCX, and RLC; and printing and plotting to Windows-certified devices. The software is made of a set of dynamic-link libraries that can be called from any Windows application. Call MDI at (407) 422-0014. *RN* **CIRCLE 662**

GREEN CHIPS MANAGE INTEGRATED POWER

Energy-efficient "green" members were added to the AM486 CPU family from Advanced Micro Devices, Austin, Texas. The chips include 66- and 50-MHz versions of the clock-doubled Am486DXL CPUs, and a 40-MHz version of the AM486DXL. All include integrated power management and the system-management mode plus processor clock control. As a result, a previously designed clock-doubled 66-MHz system (with no power management) that consumed 100 W dissipates under 30 W when idle. Support energy-saving chip sets and BIOS software are available from various members of AMD's Fusion PC alliance program—ALi, ACC Micro, PicoPower, and VIA for silicon; American Megatrends, Award, and Phoenix Technology for BIOS software. The 40-MHz CPU comes in a 168-lead PGA and costs $247 each in 1000's; 50- and 66-MHz clock-doubled versions are $268 and $357 each, respectively, in similar lots. Call (512) 602-4360. *DB* **CIRCLE 663**

LOW-MEMORY-FOOTPRINT OPERATING SYSTEM

Greater compatibility with MS-DOS is provided by ROM-DOS 6 (versus the ROM-DOS 5) from Datalight, Arlington, Wash. The low-memory-footprint (45-kbyte kernel and 27-kbyte command processor) operating system is the equivalent of MS-DOS 6.2. Aimed at handheld terminals, PDAs, and embedded computers, it supports Microsoft's Windows 3.1 and has improved LAN support. The operating system features advanced power management for systems that include the APM BIOS routines, an extended memory handler (HIMEM.SYS) to support large address spaces, and multiple CONFIG.SYS options. The latter helps developers reduce memory overhead or load different device drivers for multiple-purpose systems. Double-byte characters for Asian languages, plus functions such as Country, KEYB, and Display, are also supported for 26 languages. Through an agreement with Stack Electronics, Datalight offers Stacker 3.0 data-compression software with ROM-DOS 6 ($3 to $10 per copy for licenses under 20,000 units). The ROM-DOS 6 developers' kit costs $495. Licenses are $2 to $25 per copy. Licensees of previous ROM-DOS versions get free upgrades to ROM-DOS 6. Call Tim Gillman, (206) 435-8086. *DB* **CIRCLE 664**

VERILOG PACKAGE AIMS AT PC-BASED ENGINEERS

A new Verilog design package from Automata Publishing, San Jose, Calif., consists of a PC-based Verilog simulator, the book *Digital Design and Synthesis with Verilog HDL*, a waveform viewer, a built-in schematics checker, and 90 days of customer support. The $1000 package is aimed at engineers who need Verilog for commercial designs on a PC. The Viper/DOS simulator is a 32-bit application that runs on 80386-, 80486-, and Pentium-based machines. Viper/DOS is a true clone of Cadence's Verilog-XL simulator with respect to the language, system commands, and command-line usage. It supports version 1.0 of the Verilog language reference manual from Open Verilog International. Call (800) 884-7371 or (408) 255-0705. *LM* **CIRCLE 665**

Edited by Clifford Meth

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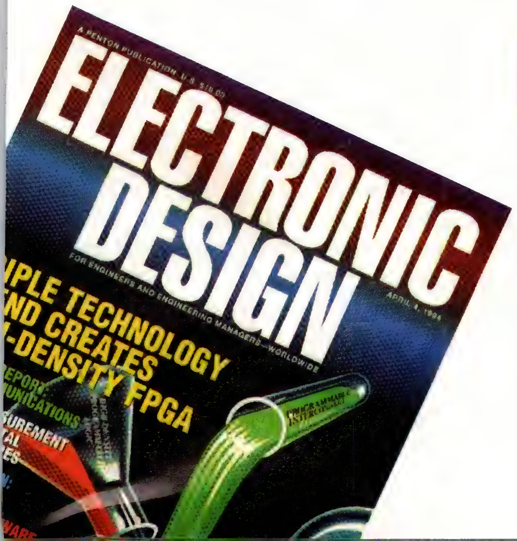

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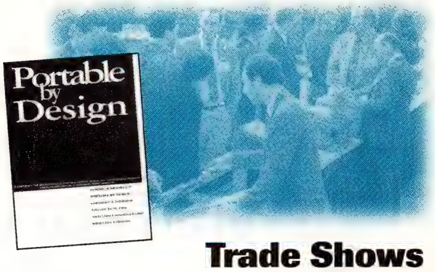

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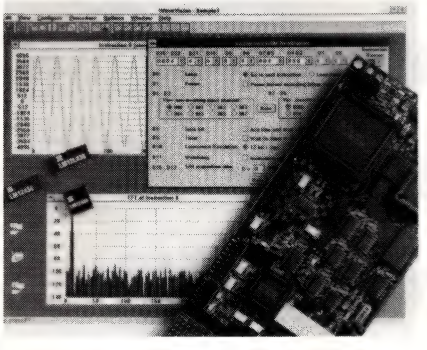
FASTEST 12-BIT DATA-ACQUISITION SYSTEM INTEGRATED CIRCUITS FEATURE GLUELESS SERIAL INTERFACE

It wasn't long ago that a 12-bit data acquisition system (DAS) filled a good sized pc board. It poked along at 25 to 50 kHz, needed 10 or more watts of power from ±15-V rails, and could cost hundreds of dollars.

About two years ago, National Semiconductor announced a complete 12-bit-plus sign, parallel output, data-acquisition system on a single CMOS chip—the LM12454. Now, adding to that family, are a pair of serial I/O versions, the four-channel LM12434, and the eight-channel LM12{L}438. These offer throughput/sampling rates of 140 kHz and 105 kHz, respectively. Not only are these the fastest 12-bit, serial I/O data-acquisition systems available, but also they interface with virtually all common microprocessors, DSPs, and serial busses. These include Intel's 8051, the Hatachi's SCI, TI's TMS320 family, National's Microwire/PLUS, and Motorola's SPI/QPSI. In addition, they are the first 12-bit ADCs compatible with the I_2C bus, which provides true two-wire communications. Maximum power drain from a 5-V rail runs less than 45 mW, and they sell for under $20 each (less than the cost of 12-bit IC ADCs just a few years ago).

The LM12434 and LM12{L}348 combine their input multiplexer with a sample-and-hold amplifier, and a 12-bit-plus-sign ADC. The ADC feeds a 16-bit-wide FIFO, which can store up to 32 data words. The FIFO gets its instructions from, and feeds data to, an on-chip bus, which in turn interfaces with the serial I/O. The software-programmable flexibility of these data-acquisition systems is remarkable. Programmable functions, the instructions for which are downloaded into an on-chip RAM or registers via the I/O, include:

- Single-ended or differential inputs for the multiplexer of the LM12{L}348 (the LM12434 has four differential inputs).
- Conversion sequencing of the multiplexer for up to four or eight conversions, respectively, by the LM12434 or LM12{L}348.



- Operation in any one of three modes: 12 bits plus sign (13 bits), 8 bits plus sign (9 bits), 8 bits plus sign comparison, or "Watchdog."
- "Watchdog-mode" mode limits.
- The sample-and-hold amp's acquisition time/data-acquisition system throughput rate.

The trio of operational modes represents one of the most unique features of this family. While in the 9- and 13-bit modes, the chip's ADC performs complete conversions with 9- or 13-bit resolution and "no-missing-code" accuracy; in the Watchdog mode, the ADC checks to see if the input is within some preprogrammed pair of high and low values (limits) with 9-bit accuracy. If these limits are exceeded, a flag is raised and sent to the host via the I/O. The host can then direct the data-acquisition system to make a conversion on that particular channel to 9- or 13-bit accuracy. Because maximum conversion time in the 13-bit, 9-bit, and Watchdog modes run 7.3, 3.5, and 1.8 μs, respectively, the DAS can be set up to monitor inputs at high data rates and only take data if the limits are exceeded.

The ADC is a true sampling converter and ac specifications are provided on the data sheet. For example, while differentially sampling a 62-kHz input at 133-kHz signal-to-noise ratio = 70 dB, (signal-to-noise + distortion) ratio = 67 dB, Total harmonic distortion = –71 dB, effective number of bits (ENOB) = 12.1, and Spurious free dynamic range = 76 dB.

The LM12434 and the LM12}438 come in 28-pin PLCCs and wide-body SOICs. Pricing in quantities of 1000 starts at $18.90 each for the LM12434, and $16.60 each for the LM12}438.

National Semiconductor, P.O. Box 58090, M/S 16.300, Santa Clara, CA 95052.8090; Rich Wegner, (408) 721-5831.

CIRCLE 800

■ FRANK GOODENOUGH

SENSOR HANDLES -50°C TO +150°C

The AD22100 IC temperature sensor needs no negative supply rail to measure temperatures below 0°C—it handles temperatures from –50°C to +150°C. The inexpensive IC, which runs as low as $0.98 in lots of 1000, is designed to replace thermistors and even thermocouples in a wide range of equipment and systems—particularly those already employing microcontrollers sporting on-chip 8-bit a-d converters. The AD22100 employs ratiometric techniques using the positive supply rail as its reference. Thus, its output voltage equals the temperature sensed multiplied by the supply voltage. The temperature sensor's nominal output signal range runs from 0.25 V to 4.75 V, making it a good match for an a-d converter with a 0-to-5-V input voltage range. The sensor nominally operates from supply rails between 4 and 6 V, from –50°C to +150°C. Operation from a 3-V rail is possible if measuring temperatures above 0°C. The sensor comes in either a 3-pin TO-92 or an 8-pin SOIC. Three accuracy grades guarantee a maximum error over three temperature ranges: The K-grade holds within ±2.0°C from 0°C to +100°C; the A-grade holds within ±3.7°C from –40°C to +85°C; and the S-grade holds within ±4°C over the full 200°C range. Prices are $0.98 to $1.32 each in lots of 1000.

***Analog Devices, Inc.,** 181 Ballardvale St., Wilmington, MA 01887; (617) 937-1428; fax (617) 821-4273* CIRCLE 801

■ FRANK GOODENOUGH

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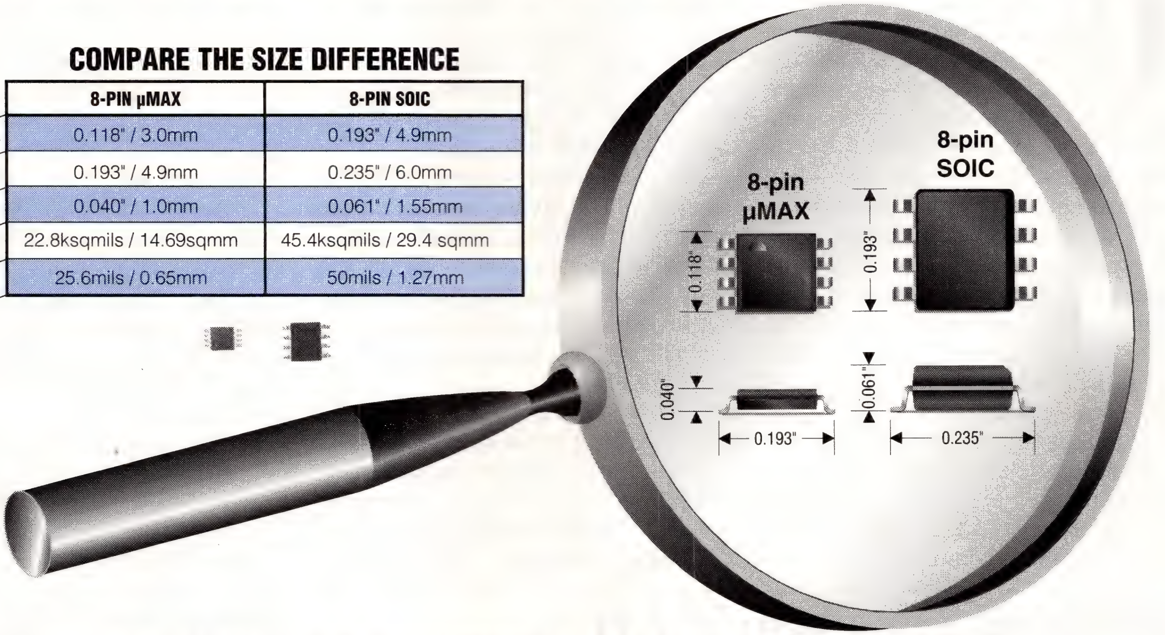

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READER SERVICE 140

FAST-TURN LASER-PROGRAMMED GATE ARRAYS PACK FROM 20K TO 45K GATES

Upping the density of their laser-programmed gate arrays, Chip Express now offers a 0.8-µm family that has complexities ranging from 20k to 45k total gates, and up to 300 programmable I/O lines. Fabricated with a double-level metal process, the arrays can be customized, packaged, and shipped in as little as one working day (more typical is three to five working days). That allows designers to quickly get prototypes and trim weeks off the wait for mask-programmed arrays.

The high-density family offers internal toggle rates of 460 MHz for flop-flops, and NAND gate delays of less than 300 ps (fanout of 1). This is about twice as fast as the company's previously-released 1.2-µm array family, and about twice as fast as most field-programmable gate arrays. The higher speed of the QYH500 arrays suites them well for evaluating timing-critical circuits that cannot easily be modeled or emulated with FPGAs. Once the design is verified, metal-mask versions (the One Mask option) can be ordered through Chip Express's partner, Yamaha Corp., San Jose, Calif., to lower production costs.

Arrays in the QYH500 series come in three gate capacities—20k, 30k, and 45k gates and are supported by the company's QuiCk place and route software and proprietary laser programming systems. The software accepts design files from industry-standard design tools, from companies such as Mentor, Synopsys, ViewLogic, and Verilog. Once the place and route software generates the "cut list," a 45k-gate chip can be configured in about two hours.

Non-recurring engineering charges start at $12,500 for the QYH520 (20k gates), which includes two fully tested parts. In lots of 10,000, the 2-kgate chip in a 128-pin PQFP sells for about $21 each. Samples of the 45k gate array are ready for configuration.

Chip Express Inc., *2903 Bunker Hill Ln., Ste. 105, Santa Clara, CA 95054; Zvi Or-Bach, (408) 988-2449.* CIRCLE 802

■ *DAVE BURSKY*

EEPROM ADDS SERIAL I/O FOR VESA DDC INTERFACE

Providing a single-chip support solution for the intelligent monitor data-display channel (DDC), the 24LC21 EEPROM from Microchip can monitor the data-display channel interface and upon power-up will send a 128-byte extended display ID (EDID) message to the host-system controller.

The DDC standard is fostered by the Video Equipment Standards Association (VESA), San Jose, Calif., and uses a two-wire bidirectional interface employing the inter-IC communications protocol.

When installed in a monitor, the 24LC21 will detect an input pulse from the DDC-compliant host-PC graphics controller, when the controller is first powered up. A vertical synchronization pulse on the memory's Vertical Clock pin puts the chip into the DDC1 serial-transmit-only mode.

A subsequent pulse on the Serial Clock pin actuates the DDC2B bidirectional communication mode. In either case, the chip immediately sends its 128-byte EDID packet when it senses a pulse. This packet contains all the data required to automatically identify the monitor and configure the controller for that monitor.

Thus, without adding a microprocessor or other circuitry, the 24LC21, which is housed in an 8-lead plastic miniDIP or SO package, makes it easy to add basic compliance to the VESA DDC standard. By installing and then programming the memory in the monitor at the factory as the last step in the production line, manufacturers have the flexibility of determining the monitor characteristics during final testing.

In contrast, suppliers that implement the EDID code as part of a microcontroller's firmware will be forced to inventory multiple chip options to support several monitor types.

Priced at just $0.71 each in lots of 10,000 units, the 1-kbit (128 words by 8 bits) EEPROM draws just 1 mA from 2.5-to-5.5-V supplies. Samples are immediately available.

Microchip Technology Inc., *2355 West Chandler Ave., Chandler, AZ 85224-6199; Nathan John, (602) 786-7200.* CIRCLE 803

■ *DAVE BURSKY*

WIDE-WORD SRAMS FOR MID-SPEED SYSTEMS

Available with a 64-kword-by-16-bit organization, the M5M51016ALL or 51016AL 1-Mbit static RAMs are aimed at systems that require access times of 70, 85, or 100 ns. The moderate-speed SRAMs satisfy the growing wide-word needs of systems that operate with 10- to 15-MHz bus-transfer rates. The ultra-low-power AAL suffix version draws a standby current of just 10 µA, maximum (1 µA, typical), from a 3-V power supply, while the standard version, the AL suffix device draws about 50 µA from a 3-V supply.

Furthermore, the chips have a data-retention mode that will hold data in the memory cells even with supply levels of as little as 2-V. Active currents are 100 mA, maximum (70 mA typical) for either version. Housed in a 44-lead standard or reverse pinout (good for layouts with memories on both sides of a circuit board), both versions, with commercial (0-70 °C) operating temperature ranges sell for $15.75 each in lots of 10,000 units. An extended-temperature-range (-40 to +85 °C) version sells for $19.75. DB

Mitsubishi Electronics America Inc., 1050 East Arques Ave., Sunnyvale, CA 94086; (408) 730-5900. CIRCLE 804

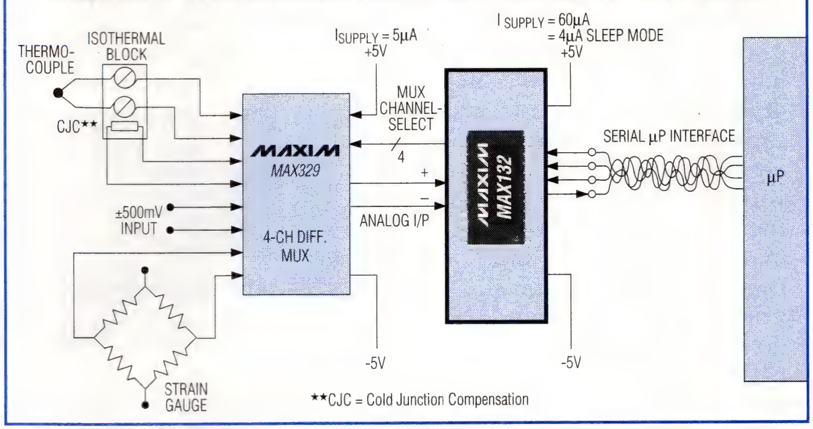
±18-BIT SERIAL ADC USES ONLY 60µA

Interface Directly to Your Transducer for only $8.00*!

Maxim's new MAX132 ADC delivers 2µV resolution, dissipates only 1mW max over temperature, and saves even more power with its 4µA sleep mode. A serial interface reduces board space and allows for inexpensive isolation. And if your application calls for multiple input channels or programmable gain, the MAX132's four digital outputs remotely control a MUX or PGA via the serial interface, eliminating extra "glue" logic and serial control lines.

- **2µV Resolution at ±500mV Full-Scale**
- **Supply Current Over Temperature:**
  - **Operating Mode: 60µA 125µA Max**
  - **Sleep Mode: 4µA 10µA Max**
- **Up to 100 Conv/sec Throughput**
- **4 Serially Programmed Digital Outputs for Remote Control of MUX/PGA**
- **±10pA Input Current**
- **50/60 Hz Rejection**
- **Space-Saving 24-Pin DIP and SO**
- **Parallel Interface Version Available – MAX135**

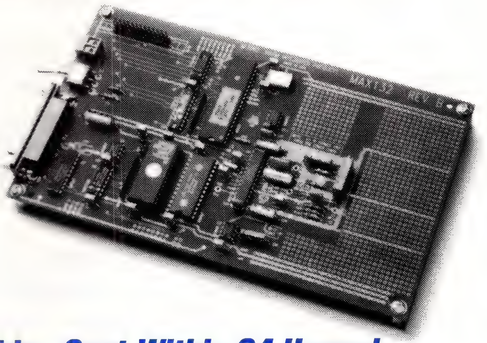
SIMPLIFY THERMOCOUPLE AND BRIDGE INTERFACING

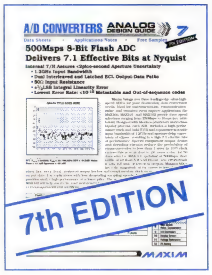


Benefit from the MAX132's high resolution, low noise, and 10pA input current by interfacing directly to transducers and other low-level signals.

Complete Kit Speeds Evaluation, Reduces Design Time

A pre-engineered MAX132 Evaluation Kit and your personal computer can save you hours of component gathering, board assembly and evaluation time. The kit contains a pre-drilled board and all the components needed to build a complete, high-resolution ADC circuit plus application-specific software and an RS-232 interface for your PC.
Call 1-800-998-8800 and order MAX132EVKIT, for $95†.





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500Msps 8-Bit Flash ADC
Delivers 7.1 Effective Bits at Nyquist
Internal T/H Assures <2pico-second Aperture Uncertainty
- 1.2GHz Input Bandwidth
- Dual Interleaved and Latched ECL Output-Data Paths
- 50Ω Input Resistance
- ±1/2LSB Integral Linearity Error
- Lowest Error Rate: $<10^{-15}$ Metastable and Out-of-sequence codes

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READER SERVICE 141

SOFTWARE EASES VXIBUS SYSTEM CONFIGURATION

The HP VXI installation software uses step-by-step on-screen instructions to help operators install and update VXIbus systems quickly and accurately. Users first tell the program what modules—including instruments, switches, mainframes, and command modules, regardless of vendor—are to be used. The software then presents logical-address settings and slot locations in a diagram that can be edited. The program graphically shows the user how to set each card's logical-address switch and the slot in which the card belongs. The user can then connect the computer to the VXI system with an included RS-232 cable, and the software will verify that the installation is correct and download needed standard commands for programmable instruments (SCPI) drivers. The program runs on PC-compatible computers under Windows 3.1. The HP VXI installation software comes with all HP E1406A command modules and HP E1300A/01A Series B mainframes. JN

Hewlett-Packard Co., Direct Marketing Org., P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844, ext. 8282. **CIRCLE 805**

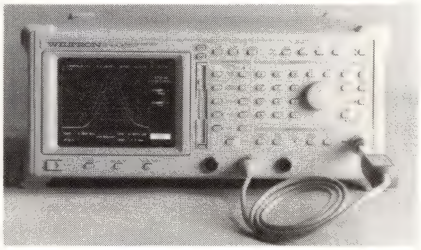
PARTIAL SCAN ATPG TOOL IS PERFORMANCE-DRIVEN

A performance-driven partial-scan capability has been added to the Aida II automatic test pattern generation (ATPG) software. The new capability selects the optimum locations for scan insertion based on performance versus area tradeoff data provided by timing-critical paths. Unlike traditional approaches, Aida II starts with 100% scan and reduces the number of structures to balance test quality against system performance and silicon area. Also added was sequential ATPG for designs containing RAMs and areas of non-scan. Other features include path delay tests and non-scan elements, dynamic vector compaction, distributed simulation, diagnostics, and support for stuck-at and I_{DDQ} testing. Aida II is available for Sun Sparcstations and Sparcserver systems and HP 9000 Series 700 workstations. Prices start at $49,000 per copy. JN

CrossCheck Technology Inc., 2833 Junction Ave., Suite 100, San Jose, CA 95134; (408) 432-0907. **CIRCLE 806**

SCALAR ANALYZER TESTS COMPONENTS TO 110 GHZ

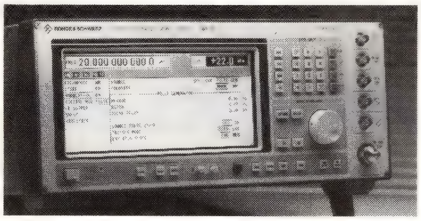
The 54100A scalar-measurement system performs scalar analysis on a variety of common production devices, including rf, microwave, millimeter-wave, and optical components. The instrument, which is suitable for benchtop or ATE environments, comes in 11 models covering frequency ranges of 1 MHz to 1.5 GHz on up to 17-26.5 GHz. Using frequency multipliers, the 54100A can do analysis to 110 GHz. The units offer fault-location software and data storage to a 1.44-Mbyte DOS disk. Automated cursor search functions and data file Auto-Name capability help simplify measurements. Model 54100A prices range from $12,300 to $60,000. Delivery is in 12 weeks. JN



Anritsu Wiltron Sales Co., 685 Jarvis Dr., Morgan Hill, CA 95037-2813; (408) 776-8300. **CIRCLE 807**

MICROWAVE GENERATORS TEST COMM EQUIPMENT

With an operating range of 10 MHz to 20 GHz, the SMP 02 and SMP 22 microwave signal generators are suitable for testing all types of communications systems. The SMP 02 has an output of up to +10 dBm and the SMP 22 output extends to +20 dBm. Both units have a harmonic supression of –50 dBc, nonharmonic suppression of –60 dBc, and SSB phase noise of –92 dBc/Hz at a 10-kHz offset from 10 GHz. Frequency resolution is 0.1 Hz. Modulation capabilities include am from dc to 250 kHz, fm from dc to 1 MHz, phase modulation from dc to 100 kHz, and pulse modulation with an on-off ratio of more than 80 dB. The instruments are made by Rohde & Schwarz and sold in North America by Tektronix. The SMP 02 costs $26,500, and the SMP 22 is $34,150. Delivery is within 10 weeks. JN



Tektronix Inc., Test and Measurement Group., P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200. **CIRCLE 808**

PROGRAMMER SUPPORTS 110 NEW DEVICES

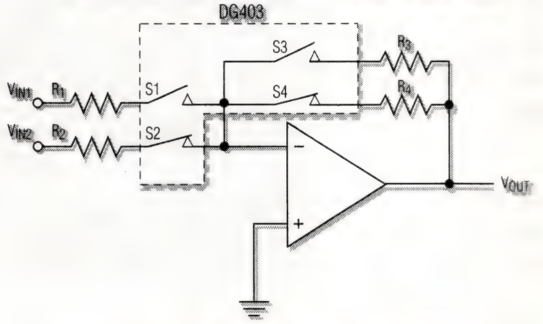
Version 1.2 of the ChipLab Project Programmer adds support for 110 more devices and offers enhanced algorithm support for more than 190 devices. The new devices supported include microcontrollers from Intel, Microchip, Philips, and Waferscale; programmable logic from Advanced Micro Devices, Cypress, and Lattice; and memory devices from AMD, Atmel, National Semiconductor, SGS Thomson, and Toshiba. Other enhancements include expandable RAM, the ability to save system settings, and improvements in memory editor operations. Boot time is shorter, and opening files, viewing data, and editing can be done faster. ChipLab costs $895 in the 32-pin version and $1495 in the 48-pin version. The version 1.2 software is available as an upgrade for $125. JN

Data I/O Corp., 10525 Willows Rd. N.E., P.O. Box 97046, Redmond, WA 98073-9746; (800) 332-8246 or (206) 811-6444. **CIRCLE 809**

IMPROVED DG400 SERIES GUARANTEES 3Ω *MATCHING* & *4Ω R_{ON} FLATNESS* FOR FREE!

The Only DG400s with Guaranteed Charge Injection

PROGRAMMABLE GAIN AMPLIFIER



Switching into a virtual ground reduces distortion caused by $r_{DS(ON)}$ variation over the analog signal range. Guaranteed $r_{DS(ON)}$ matching (typically 0.5Ω) ensures gain accuracy of <0.01% when R1 through R4 are greater than 10kΩ.

Maxim's new, improved DG400 series of switches are upgrades to industry-standard DG400 devices. These devices meet all original DG400 specifications. Their tested parameters for RON matching and flatness have never before been guaranteed. These new specifications assure lower distortion and improved linearity and accuracy for attenuators, tuned filters, sample and hold, and programmable-gain amplifiers. All switches operate over a wide supply voltage range of 10V to 30V or ±4.5V to ±20V.

ONLY MAXIM OFFERS IMPROVED PARAMETERS ON ALL DG400 FAMILY PARTS

IMPROVED PRODUCT	R_{ON} MATCH (Ω)	R_{ON} FLATNESS (Ω)	Q_j (pC)	OFF LEAKAGE at +85°C (nA)	ON LEAKAGE at +85°C (nA)
DG401/3/5	2	3	15	5	10
DG411/2/3	3	4	10	5	10
DG417/8/9	3	4	10	5	10
DG421/3/5	3	4	10	5	10
DG441/2/4/5	3	9	10	5	10

- **Guaranteed On Resistance Match Between Channels (3Ω)**
- **On Resistance Flatness (4Ω) Over Signal Range**
- **Guaranteed Low Charge Injection (as low as 10pC)**
- **4 Times Less Leakage Over Temp (less than 5nA at 85°)**
- **Guaranteed ESD Protection (>2kV) per MIL-STD-3015.7**

MUX & SWITCH ANALOG DESIGN GUIDE 1

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On-Resistance Matching and Flatness, Plus Guaranteed Low Charge Injection

FUTURE PRODUCTS New Quad SPST Low-Voltage Switches Offer +5V, ±5V Operation

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DC-PLASMA DISPLAY BOASTS SMALL PACKAGE

The smallest member of a graduated 64-by-128 series of dc-plasma displays, the GD-064X128-03 promises a wide viewing angle, long life expectancy, bright neon-orange color, and high contrast. The display is available as a glass display only, or as a glass display with attached driver electronics, control electronics, and/or dc-dc converter, the GD-064D128-03. With an active area of 3.16-by-1.92 in., and pixels arranged as 64 rows and 128 columns, the dc-plasma display boasts 8 rows of 21 characters measuring 0.19 in. in height using a 5-by-7 dot-matrix format. Also, by addressing individual pixels or groups of pixels, graphic images or larger text formats may be displayed. As an assembled module, the glass/driver option is available for $150 each. CA

Babcock Display Products, 1051 S. East St., Anaheim, CA, 92805-5799; (714) 491-5100. **CIRCLE 810**

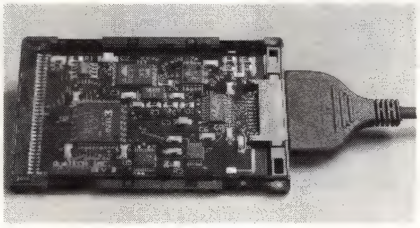
BUNDLES FEATURE QUAD CD-ROM DRIVE

Two multimedia packages bundle the SuperQuad quadruple-speed CD-ROM drive from Teac America. The first adds a removable IDE hard-disk drive that boasts a capacity of 540 Mbytes. It is priced at $1499. The second offers the FD05 0.5-in.-high floppy-disk drive. It sells for $750. The CD-ROM drive features a 600-kbyte/s data-transfer rate and an access time of 195 ms. It's 100% compatible with Sound Blaster audio boards. Both packages are available now. RN

Teac America Inc., 7733 Telegraph Rd., Montebello, CA 90640 (213) 726-0303. **CIRCLE 811**

RS-232 CARD FITS PCMCIA FORM FACTOR

The SSP-100 is a single-channel RS-232 asynchronous serial-adapter PCMCIA card that fits the Type II form factor. The card automatically configures itself upon insertion or initial system boot-up. By default, the card is assigned to the lowest available communications port. However, users can select an alternate port. A client software driver that's compatible with the PCMCIA Card Services Specification 2.1 is included with the card. As a result, the card can be removed or inserted from a live system without causing an error. Available now, the SSP-100 RS-232 adapter card costs $229. RN



Quatech Inc., 662 Wolf Ledges Pkwy., Akron, OH 44311; (216) 434-3154. **CIRCLE 812**

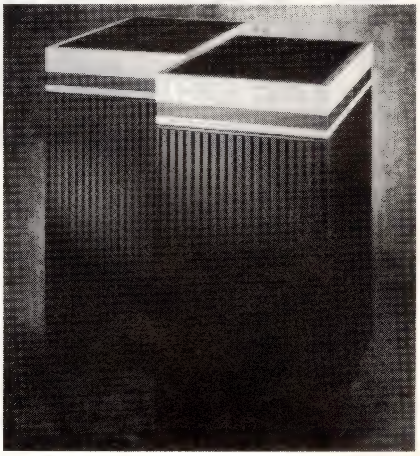
2.5-IN. DRIVES RAISE TOLERANCES

Higher capacities and shock resistances highlight a new line of 2.5-in. hard-disk drives. Using the proprietary ImpacSafe technology, the drives are able to withstand operating shocks of 100 Gs and non-operating shocks of 150 Gs. The capacities of the IDE family are 340, 510, and 680 Mbytes. The drives offer a data-transfer rate of 23 to 39 Mbits/s, an average seek time of 12 ms, an interface transfer rate of 8 Mbytes/s, and an MTBF rating of 300,000 hours. The 340-Mbyte model employs two platters and measures 12-mm high. The 510-Mbyte three-platter drive and 680-Mbyte four-platter models are 19-mm high. The 340- and 510-Mbyte drives, priced at $499 and $599 respectively, are sampling now with production expected to start by the end of the summer. The 680-Mbyte drive will sample by the end of the summer and go into production in the fourth quarter. It will cost $699. RN

MiniStor Peripherals Corp., 2801 Orchard Pkwy., San Jose, CA 95134; (408) 943-0165. **CIRCLE 813**

SUPERCOMPUTERS ARE COOLED WITH FORCED AIR

The C Series of supercomputers employs gallium-arsenide technology to perform better than 1 BOPS/CPU. This is a level that previously could only be achieved by expensive liquid-cooled systems. The C4/XA, which employs forced-air cooling, is the most power platform in the family. It combines binary compatibility and architectural extensions for increased vector performance. The C4/XA features open-system functionality, such as IEEE-based floating-point hardware, which is required for interaction with workstations, various system software, software-development tools, and a library of third-party application tools. The GaAs-based non-blocking crossbar and Automatic Self-Allocating Processors (ASAP) permit efficient parallelization without reducing overall system throughput in multi-job environments. The maximum configuration contains four CPUs and 4 Gbytes of memory. In one clock cycle, a CPU can perform twelve 32-bit vector floating-point operations or six 64-bit vector operations. RN



Convex Computer Corp., 300 Waterview Pkwy., Richardson, TX 75080; (214) 497-4000. **CIRCLE 814**

LCD WITHSTANDS EXTREME TEMPERATURES

With its low power consumption and wide operating temperature range, the G191D LCD is suited for such portable applications as medical, industrial, and test instrumentation. The 192-by-192-pixel display can operate from –20 to +70°C. Weighing about 75 g, it measures 86-by-95-by-7 mm. The viewing area is 67.4-by-67.4 mm. Typical power requirements are $V_{DD} = +5$ V at 6.5 mA and $V_{LC} = -24$ V at 6.0 mA. The display is available in an optional transreflective LED backlit version for direct sunlight applications. In quantities of 100, the G191D sells for $101. RN

Seiko Instruments Inc., 2990 West Lomita Blvd., Torrence, CA 90505; (310) 517-7770. **CIRCLE 815**

WORKSTATIONS HARNESS ALPHA MICROPROCESSORS

The Alpha processor, from Digital Equipment Corp., is starting to make a presence in the workstation market. Three vendors recently released platforms that employ the high-end RISC CPU—Carrera Computers, Neko Tech, and Aspen Systems.

The Cobra AXP 275 from Carrera is designed with the Alpha AXP 21064A chip, which runs at 275 MHz. In addition to the high-speed microprocessor, the system is based on the PCI local bus. The AXP 275 can handle the growing demand for multitasking, multiuser operating systems such as Windows NT for applications like CAD, CAE, and desktop publishing. Other features include 128-bit processor and memory buses, two PCI slots and three ISA expansion slots. Embedded on the motherboard are devices for SCSI-2, Ethernet, a parallel and two asynchronous serial ports, a floppy-disk drive, and a keyboard and mouse.

The Aspen Systems' platform also incorporates the 275-MHz Alpha chip. The Alpine motherboard fits a baby AT (8.8 by 13 in.) form factor. The board was built with upgradability in mind. As a result, users can start with a 166-, 200-, or 233-MHz processor, then upgrade later simply by replacing the CPU and clock chip. To raise performance, a secondary 2-Mbyte cache RAM comes standard. The board also contains all the conventional I/O interfaces. System memory can be expanded to 512 Mbytes using 72-pin SIMMs.

The Mach 1 and 2 systems from Neko Tech are aimed at multimedia and client-server applications. The Mach 1 is an entry-level platform that's built with a 166-MHz processor on a half-size AT motherboard. System memory ranges from 16 to 256 Mbytes. It also comes with a floppy-disk drive and a high-capacity hard-disk drive. The Mach 2 contains the 210-MHz Alpha chip, and is upgradable to 225, 275, or 320 MHz. The board is a full-size AT form factor with 128-bit interleaved error-correcting cache. System memory ranges from 16 to 512 Mbytes. It also comes with a floppy- and a hard-disk drive, and a color monitor.

***Aspen Systems Inc.**, 4026 Youngfield St., Wheat Ridge, CO 80033; (303) 431-4606.* **CIRCLE 816**

***Carrera Computers Inc.**, 23181 Verdugo Dr., Suite 105A, Laguna Hills, CA 92653; (714) 707-5051.* **CIRCLE 817**

***Neko Tech Inventory Conversion Inc.**, 9272 Jeronimo Rd., Suite 115, Irvine, CA 92718; (714) 580-0055.* **CIRCLE 818**

■ *RICHARD NASS*

Accurate to a T ...
as well as B, E, J, K, R, and S type.

For your difficult temperature monitoring problems, the SR630 Thermocouple Monitor provides the power and flexibility you need. The SR630 interfaces 7 types of thermocouples, 16 independent channels of data and easily handles monitoring and logging functions as well as computer interfacing. And the easy to use front panel makes setup a snap.

And the price? At $1495, the SR630 is the complete, low cost solution you're looking for.

The SR630 Thermocouple Monitor $1495

- 16 channels
- 0.1 degree resolution
- B, E, J, K, R, S, and T type thermocouples
- °C, °K, °F, and mV dc readings
- 2000 point non-volatile memory
- 4 proportional analog outputs
- Audible alarm
- GPIB, RS232 and Printer interfaces

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READER SERVICE 178

24-BIT SCSI FRAME-GRABBER ADDS DSP

By combining a 24-bit SCSI frame grabber with a DSP image processor, the DASM-VIP video image processor can acquire, process, and display both monochrome and color video images. The two-in-one device is built with a TI TMS320C31 DSP to help lower the total system cost for such applications as machine vision, military and defense imaging, manufacturing inspection, and security and surveillance. By emulating a SCSI drive, the DASM-VIP can be connected directly to most platforms.

With up to 16 Mbytes of memory, the device can capture real-time video data from various sources, including RGB, NTSC, and S-Video color and RS-170 monochrome sources. A proprietary digital sync-lock circuitry virtually eliminates pixel jitter to increase the accuracy of image data from noisy sources. The video images can be displayed as either a single frame or as a sequence of real-time frames. In addition, the DASM-VIP's external trigger input can be controlled by external events, and an external clock input is provided for cameras with pixel-clock outputs.

The 33-MFLOPS DSP chip relieves the host CPU from the imaging tasks. DSP application programs, downloaded to the peripheral, can perform such tasks as frame averaging, edge detection, and filtering. A real-time operating system resides in the DASM-VIP to simplify code writing. Additional software support includes TI's TMS320 development tools and a C31 unified software development kit. Prices for the DASM-VIP start at $2995. The C31 development kit sells for $3000.

***Analogic Corp.**, 8 Centennial Dr., Peabody, MA 01960; (508) 977-3000.* **CIRCLE 819**

■ *RICHARD NASS*

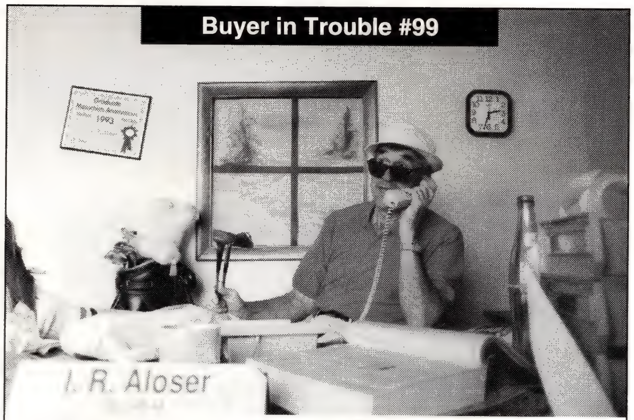
PCMCIA FAX-MODEM ADDS 4 MBYTES OF RAM

By combining 2 to 4 Mbytes of expanded memory with a fax-modem and interface software in a Type II PCMCIA card, the FMM overcomes some of the limitations of low-memory, single-slot subnotebook and palmtop computers. The card lets users access on-line services and download files without running out of system memory.

Other features of the fax-modem card include a low-power sleep mode and flash memory for software upgrades. In the sleep mode, the current draw drops to less than 2 mA. The modem operates at 2400 bits/s, while the fax sends and receives at 9600 bits/s. Available now, the FMM PCMCIA fax-modem sells for $349 with 2 Mbytes of RAM and $449 with 4 Mbytes. RN

Smart Modular Technologies Inc., 45531 Northport Loop West, Building 3B, Fremont, CA 94538; (510) 623-1231. **CIRCLE 820**

Buyer in Trouble #99



Losing the Golf War

"Rocky. This new catalog's not only got transformers, it's got golf balls guaranteed to go 400 yards. Don't scream, Rocky. I didn't know Prem had a new catalog. But think about it, Rocky, 400 yards... (CLICK!) Rocky?? Hello...Hello...
I *really* shoulda called Prem.
You oughta call Prem!"

PREM®
Where Quality Really Counts!

For Prem's new catalog or additional product information, call or write
Prem Magnetics, Inc.,
3521 North Chapel Hill Road, McHenry, IL 60050.
Phone: 815-385-2700. FAX: 815-385-8578.

READER SERVICE 104

Put Our List On Your List

Our list can help you do the other things you have on your list. Such as buy a car. . . estimate social security. . . start the diet. . . check out investments. . .

Our list is the *Consumer Information Catalog.* It's free and lists more than 200 free and low-cost government booklets on employment, health, safety, nutrition, housing, Federal benefits, and lots of ways you can save money.

So to shorten your list, send for the free *Consumer Information Catalog.* It's the thing to do.

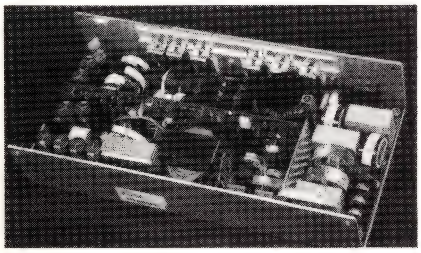
Just send us your name and address. Write:

Consumer Information Center
Department LL
Pueblo, Colorado 81009

A public service of this publication and the Consumer Information Center of the U.S. General Services Administration

500-W SWITCHERS CORRECT POWER FACTOR

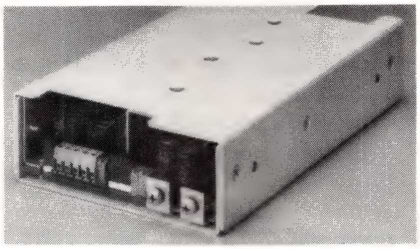
Up to four fully isolated and regulated outputs in a low-profile, 10-by-4.88-by-2.19-in. package are provided by the PX500 Series switching power supplies. With a main output rated at 5 V at 80 A, the 500-W units feature power-factor correction to 0.99, universal input, on-board FCC/VDE Class B EMI filtering, and harmonic-distortion reduction that meets IEC 555-2. N+1 and redundant applications are simplified by active current-sharing circuitry. DM



Basler Electric, Route 143, Box 269, Highland, IL 62249; (800) 645-2074. **CIRCLE 821**

SWITCHING SUPPLIES OFFER FULL FEATURE SET

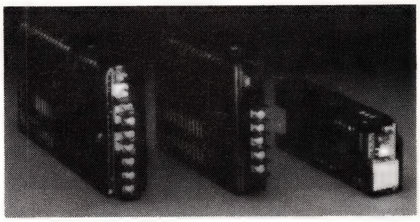
Fewer through-hole components, a smaller footprint, and a lower profile are all features of the NMX Series of switching power supplies. For example, at, 4.75 by 8 by 1.75 in., the NMX-350 occupies just 66.5 in.^{3}. Yet, the 350-W unit incorporates a full range of features including a universal ac input (90 to 264 V ac), built-in power-factor correction to 0.99, minimum rms input current, low peak-to-peak noise and ripple on all outputs, and many more. Call for pricing. DM



Todd Products Corp., 50 Emjay Blvd., Brentwood, NY 11717; (516) 231-3366. **CIRCLE 822**

COMPACT SWITCHERS PUMP UP EFFICIENCY

The HY Series of compact, lightweight switching power supplies offers a profile of less than one inch. Efficiency, however, remains high at from 77 to 85%. Models with 25-, 50- and 100-W outputs are included in the series, as are 5-, 12-, and 24-V outputs. All units have universal inputs and meet IEC 950, UL 1950, and CSA 22.2/154 specifications. They also meet FCC and VDE Class B and VCCI Class 2 emissions standards. Call for pricing. DM



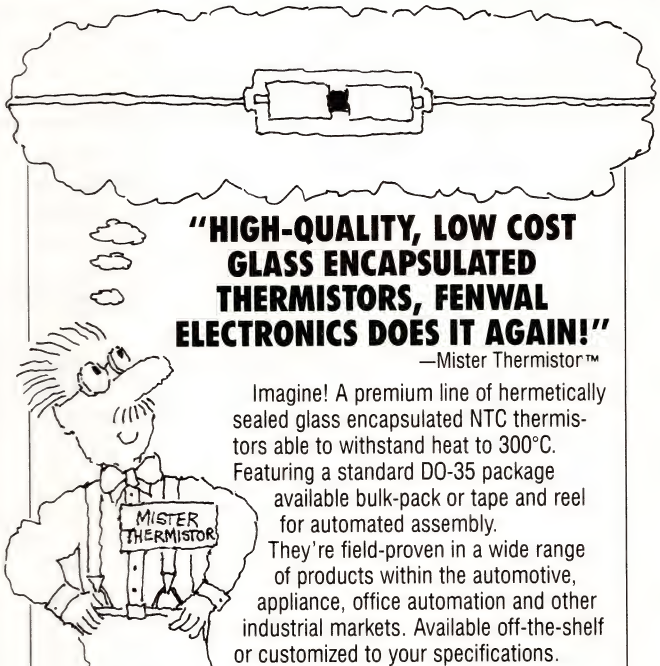
Shindengen America Inc., 2985 E. Hillcrest Dr., Suite 140, Westlake Village, CA 91362; (800) 634-3654. **CIRCLE 823**

You Need Tree City USA

City trees add the soft touch of nature to our busy lives. They cool our cities, fight pollution, conserve energy, give wildlife a home, and make our neighborhoods more liveable.

Support Tree City USA where you live. For your free booklet, write: Tree City USA, The National Arbor Day Foundation, Nebraska City, NE 68410.

The National Arbor Day Foundation



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—Mister Thermistor™

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READER SERVICE 88

Low-Cost CAD Tool Analyzes Timing

The Timing Diagrammer is a low-cost CAD tool for drawing and analyzing timing diagrams. It's used for pre-schematic and block-diagram-level analyses that help engineers decide which parts are suitable for a particular circuit. Once actual parts have been chosen, Timing Diagrammer can quickly verify circuit timing at the gate level. Timing parameters such as delays and setup-and-hold times actively move and monitor signal transitions. Parameter values are edited using a custom spreadsheet. The timing diagram automatically adjusts to reflect parameter changes. Timing Diagrammer also has features tailored for documentation. For example, the copy-to-clipboard feature lets timing diagrams and parameter data be exported to word processors and desktop publishers. Timing Diagrammer runs on PCs under Windows 3.1. It's available for a limited time at $249.99. Quantity discounts and site licenses are available. Call the company for a free evaluation diskette. LM

SynaptiCAD, P.O. Box 10608, Blacksburg, VA 24062-0608; (703) 953-3390. CIRCLE 824

Micro Channel, SCSI-2 Added To Model Family

The Logic Modeling Group of Synopsys has added Micro Channel and SCSI-2 models to its product line. The simulation model of the Micro Channel Architecture (MCA) standard is part of the SimuBus product line, which includes models of the PCI, PCMCIA, ISA, EISA, and VME standards. SimuBus MCA complies with the most recent version of the MCA specification based on the IBM-licensed technology, and has been evaluated and tested by IBM. The model consists of a set of behavioral-simulation models and control programs that can be connected together to simulate a virtual MCA system. A SCSI-2 protocol model is the newest addition to the company's family of standard interface models. The SCSI-2 model lets engineers create a "virtual system" to verify a design before prototyping. It's a complete and accurate bus-functional model of the most recent version of the ANSI specification. Master and slave modules emulate SCSI-2 initiator and target behavior. SimuBus MCA is available now for most commercial simulators. A perpetual site license costs $25,000. The SCSI-2 model is also shipping now. It supports all major Verilog and VHDL simulators, and cost $15,000. LM

The Logic Modeling Group of Synopsys Inc., 19500 N.W. Gibbs Dr., Beaverton, OR 97006; (800) 344-0004. CIRCLE 825

Layout Tool Creates Deep-Submicron ASICs

Epoch/Datapath is the newest member of the Epoch family of high-level physical design software from Cascade Design Automation. The new tool performs automatic layout of deep-submicron, datapath-based ASICs. It combines datapath-module generators, place-and-route tools optimized for datapath, and timing analysis. Epoch/Datapath is integrated with popular HDL-based CAE systems to provide a front-to-back high-level design environment. Designs that are captured, simulated, and synthesized in Verilog or VHDL are automatically turned into complete layouts. Epoch/Datapath will ship in September. Pricing starts at $80,000. LM

Cascade Design Automation Inc., 3650 131st Ave. S.E., Suite 650, Bellevue, WA 98006; (206) 643-0200. CIRCLE 826

Accelerator Speeds Fault Simulations

The Paradigm XP Super Fault hardware accelerator from Zycad delivers 20 to 120 times the speed of the fastest fault-simulation software running on a powerful workstation. This product is the latest addition to the company's Paradigm Verification workbench—a tool suite for concurrent verification of complex ASICs and systems. Zycad is also announcing a set of features that lets users more efficiently perform fault simulations on large systems, even if they include full or partial internal scan. The new features are: an interactive fault tracer, test-directed fault simulation, strobe windows, and parallel loading of scan vectors. In addition, the Paradigm XP Super Fault simulator supports concurrent simulation using accurate pin-to-pin timing, which is an important feature for the 50% of designs that contain asynchronous elements. The system provides capacity from 64,000 to 4 million gates for fault simulation, and from 256,000 to 16 million gates for logic simulation. Pricing starts at $79,000. LM

Zycad Corp., 47100 Bayside Pkwy., Fremont, CA 94538-9942; (800) 243-7286 or (510) 623-4400. CIRCLE 827

Emulation Tools Aim At Chips And Boards

The Explorer Series system-emulation products from Aptix include two separate tools aimed at ASIC- and board-level verification. Explorer ASIC is designed to emulate 30,000 gates of standard logic, plus many types of embedded cores. It operates at 10 MHz and up, can emulate all functions within an ASIC, and provides complete observability through 384 hardware probes operating under software control. Verilog net lists are partitioned and mapped to the system's internal Xilinx FPGAs. The Explorer MP3 Board Emulator runs at 50 MHz. With MP3, engineers can insert a mix of standard components for comprehensive board-level emulation. The components can include multichip modules, microprocessors, microcontrollers, RAMs, ROMs, digital-signal processors, and FPGAs. Explorer MP3 can handle multiple device types by exploiting the company's interconnect technology, which enables pin-to-pin programmability across the board. It has four 36-bit bi-directional buses; multiple low-skew buffered clock lines; and component adapters that automatically pick up power, ground, and control lines. Explorer ASIC can become part of a system-level emulation by plugging it into the actual target system, or the Explorer MP3 product. Pricing for the Explorer Series ranges from $40,000 to $80,000 in a typical configuration. That price includes all the necessary hardware and software. LM

Aptix Corp., 2890 N. First St., San Jose, CA 95134; (408) 428-6200. CIRCLE 828

ENHANCED ESDA TOOL HAS BETTER DEBUG

An enhanced version of the Visual HDL electronic-system-design-automation (ESDA) tool has an improved design and debugging environment. Other new features include the support of Unix workstations and the generation of Verilog hardware-description-language code for simulation and synthesis. Design entry now supports pre-defined datapath elements based on the LPM standard, the definition of multiple concurrent state machines within one state diagram, and tracking of the aggregate state of a simulated design. New simulation capabilities can trace the control path of the simulated design, can search for specific signal values displayed in the waveform window, and can probe and display current signal values in block diagrams during simulation. A simulation control window consolidates all commands into one location. Visual HDL has identical functionality on PC and Unix platforms. The new release of Visual HDL will ship in September for PCs and Sun workstations. Pricing is set at $12,500 and $25,000, respectively. LM

Summit Design Inc., 9305 S.W. Gemini Dr., Beaverton, OR 97005; (503) 643-9281. CIRCLE 829

VHDL EDITOR ENSURES SYNTHESIZABLE CODE

Vantage VHDL Editor is a design-entry tool that streamlines and automates the tasks of entering correct and synthesizable VHDL text, and checking multiple synthesis subsets. The editor is as easy to use as VI or Emacs text editors. It automatically performs VHDL syntax checking and structural formatting, provides customizable templates for modeling consistency, and allows for targeting of multiple synthesis tools. Vantage VHDL Editor currently supports Design Compiler from Synopsys, ASIC Synthesizer from Compass Design Automation, and ViewArchitect and ViewSynthesis from Viewlogic. The Unix-based product costs $2000. LM

Vantage Analysis Systems Inc., 47211 Lakeview Blvd., Fremont, CA 94538; (510) 659-0901. CIRCLE 830

CONCURRENT-ANALYSIS SOFTWARE EXAMINES PHYSICAL EFFECTS

A computer-aided-analysis tool suite from UniCAD called UniSolve helps engineers examine the physical effects that result from high-speed system designs. Specifically, the software analyzes electromagnetic interference (EMI), digital and analog signal integrity, thermal properties, RF and IF, and reliability. More importantly, these tools work in a concurrent environment that enables the transparent exploration of interdependencies among these effects.

UniSolve provides concurrent-engineering analysis by automatically computing the impact that a design decision in one area could have on another. For example, while analyzing the effect that grouping together noisy devices has on EMI, UniSolve will immediately indicate what thermal conditions have been generated. Algorithms for several different dependability aspects of a design are packaged together in UniSolve to give both general and expert design-experimentation capabilities.

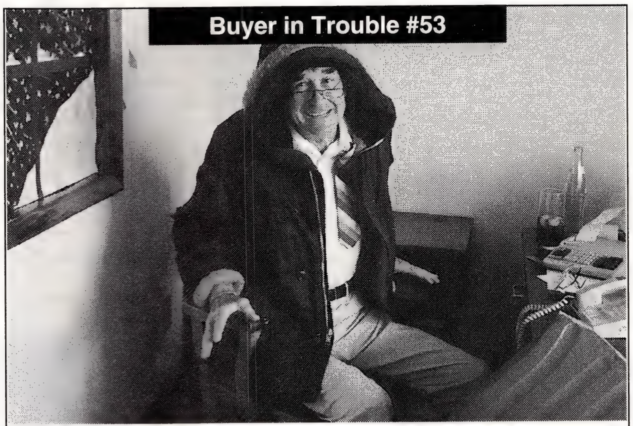
Users can see various representations of a design, such as the EM or thermal view. The toolset displays a home-base view of the design, plus a view of the design under each analysis type that's selected. As a result, users can apply multiple analyses to a design simply by selecting different views.

UniSolve will work with existing layout tools. The entire suite costs $115,000. Each tool can also be purchased separately.

UniCAD Inc., 174 Littleton Rd., Suite 103, Westford, MA 01886; (508) 692-8446. CIRCLE 831

■ *LISA MALINIAK*

Buyer in Trouble #53



Love Potion # B.S.I.

"She had beautiful eyes. She said she could design for B.S.I. Then she left me out in the cold. I'm dead meat. Prem has a whole series of transformers that already have British Standard Institute approval.

I *really* shoulda called Prem.

You oughta call Prem!"

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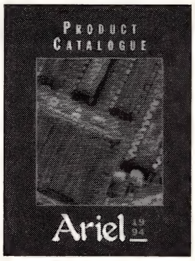
READER SERVICE 105

CATALOG/LITERATURE REVIEW

DSP and I/0 Boards/Systems

New 1994 catalog of digital signal processing boards, systems and software plus a full range of analog and digital I/O for VME, Sbus and PC/AT. Systems range from single DSPs to large-scale parallel processor solutions.

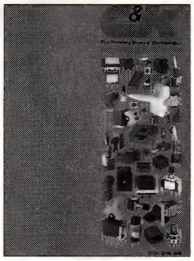


Circle 303

ARIEL CORP.

C&K's New Switch Catalog

Offering the broadest line of switch products, C&K's new Catalog #9308 provides valuable design information for wide range of applications. Complete photo descriptions and specifications, along with electrical ratings, mechanical ratings, mechanical operation characteristics are included.

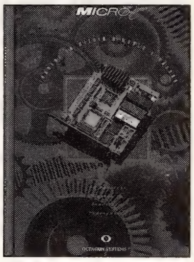


Circle 274

C&K Components, Inc.

Embedded PC Catalog

Octagon System's, Westminster, CO, 112-page catalog displays their Micro PC® family. The Micro PC line is designed for apps. where small size wide temperature range, and rugged packaging are critical. ISO 9001 certified.

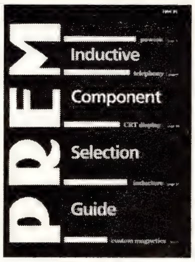


Circle 275

OCTAGON SYSTEMS

INDUCTIVE COMPONENTS CATALOG

New catalog features entire line of power transformers, telecommunication magnetics, CRT products, and inductors. Power transformers carry UL and CSA listings. International series includes UL, IEC, VDE and CSA approvals. The telecommunications line includes coupling and hybrid transformers for voice and/or data, plus many other special applications.

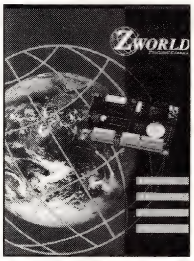


Circle 276

PREM MAGNETICS,INCORPORATED

C-Programmable Controllers

Save time and money. Our controllers are ideal for control, test or data acquisition applications with a mix of analog/digital I/O, relays, RS232/485 serial ports, LCD/keypads, & programmed with Dynamic C™. From $159, Qty. 1. (916) 757-3737, or Fax: (916) 753-5141. For 24 Hr. data, call from YOUR Fax: (916) 753-0618.

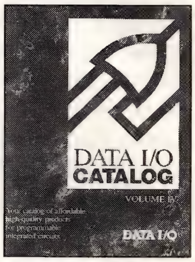


Circle 277

Z-World Engineering

MADE TO ORDER

The Data I/O catalog makes our affordable tools easy to order. Phone, Fax, or mail in your order, and we'll deliver great values on high-quality design software and device Programmers. Call today for your FREE catalog.



Circle 278

DATA I/O CORPORATION

Highspeed Waveform Capture

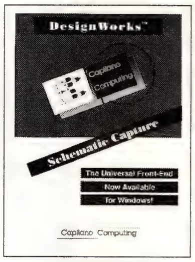
Signatec, Corona, CA. - A binder containing data sheets for all of its pc based products for use in the areas of waveform capture, waveform generation and signal processing can be obtained by contacting them at (909) 734-3001

Circle 279

Signatec Inc.

SCHEMATIC CAPTURE

This brochure details DesignWorks for Windows, the universal front end for use with PCB, FPGA, ASIC and SPICE packages. Software features full hierarchy, automatic gate packaging and 13,000 + symbols.

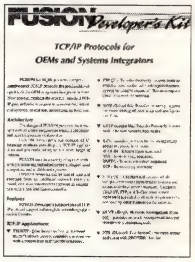


Circle 280

Capilano Computing

TCP/IP DEVELOPER KITS

Fusion is a Highly Portable set of TCP/IP protocols with the OEM or systems integrator in mind combine industry standard TCP/IP suite with your embedded system also available SNMPV.2 Network management agent code.



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Pacific Softworks Inc. sltl

DEVICE PROGRAMMERS

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PILOT Programming Instruments.
Finest Quality at Affordable Prices.
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Circle 282

Advin Systems Inc.

Device Programming Tools

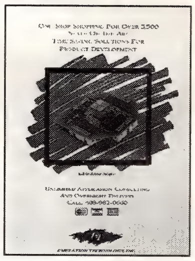
The Newest Advances are presented in over 20 pages, illustrating the widest selection of development and production tools, PLO/FPGA Design software, UV erasers, and Prom/PLD Programmers from the leading manufacturer.

Circle 283

LOGICAL DEVICES, INC.

VLSI/SMT SOLUTIONS CATALOG

Free '94 catalog. Over 3500 devices; 120 "off-the-shelf" items available for overnight delivery. Unlimited application consulting. Ask about our custom designs. Leading edge technology —over 500 PQFP Solutions. Time Saving Solutions.

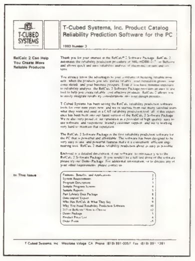


Circle 284

EMULATION TECHNOLOGY

Reliability Prediction

Catalog describes the RelCalc2 software Package, which automates Mil-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: (818) 991-0057 Fax: (818) 991-1281

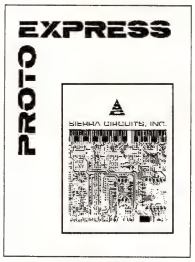

T-CUBED SYSTEMS
T-Cubed Systems, Inc. Product Catalog
Reliability Prediction Software for the PC

Circle 285

T-Cubed Systems

PROTO EXPRESS

Multilayer prototypes in 1 to 5 days. FR4 and polyimide. Commerical or Milspect capabilities *buried/blind VIAS* carbon paste* up to 22 layers. Call Ken or Joycie 408-735-7137 phone 408-735-1408.

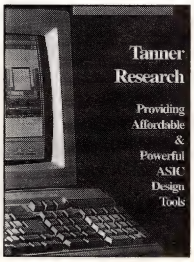


Circle 286

Proto Express

ASIC Design Software

Tanner Research, Pasadena, Calif., has a new brochure with detailed information on its complete line of affordable CAE/CAD software for ASIC design and layout. A free demo disk and price list are included.



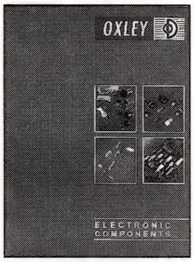
Circle 287

TANNER RESEARCH

CATALOG/LITERATURE REVIEW

ELECTRONIC COMPONENTS

1994 Catalog contains technical info on our full range of components which include: EMI/TVS Filters, Planar Arrays, Trimmer Capacitors, Led Indicators NVG Displays, Elapsed Time Indicators, Test Points for pcbs, fiber optics.

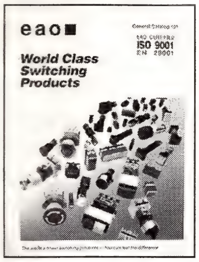


Circle 288

OXLEY INC.

EAO'S NEW FULL LINE CATALOG

Now available from EAO Switch Corporation,112 page catalog. Included are all EAO'S newest switches with product photos, features, mounting dimensions, technical information, specifications and international approvals. Organized by applications and catagories. Types of illumination, accessories, lens shapes and colors are listed.

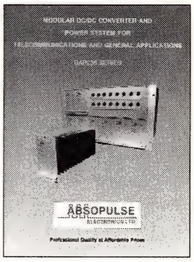


Circle 289

EAO Switch Corporation

Battery Chargers

The PFC Rectifier delivers 500W to load or Battery (2500W per rack), Features include full electronic protection, redundancy, high MTBF and hot swapping. The series is available in rack mount or stand-alone format.

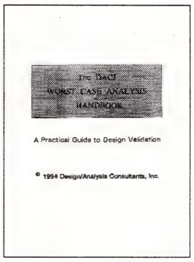


Circle 290

Absopulse Electronics

DESIGN VALIDATION

Use DACI's Handbook to achieve reliable, cost effective, optimized designs, without the need for complex math.
$49/Copy (Free with purchase of DACI's Worst Case Analyzer software.)

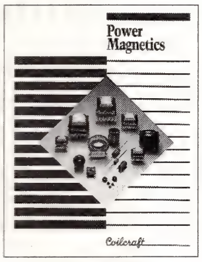

The DACI
WORST CASE ANALYSIS
HANDBOOK
A Practical Guide to Design Validation
© 1994 Design/Analysis Consultants, Inc.

Circle 291

Design/Analysis Consultants, Inc.

Power magnetics featured

New 48-page catalog includes surface mount magnetics, switching power transformers, output filter chokes, current sensors, common mode line chokes, and variety of other devices. Also covered are Coilcraft's designer's kits that speed prototyping.

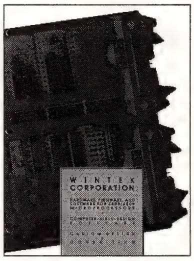


Circle 292

Coilcraft

Microcomputer Modules & CAD

The catalog describes 6800 and 6809 single-board computers, input/output interfaces debuggers, compilers and assemblers; plus schematic capture and printed circuit board layout software and accessories for the IBM personal computer.

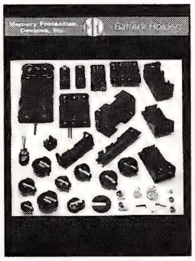


Circle 293

Wintek Corporation

BATTERY HOLDERS

Featured products: SMT button cell holders, battery snaps, case hardware, computer clock back-up holders, multi-cell holders with covers, auto cigarette lighter plugs. For computers, alarms, controls, instruments, toys, appliances, etc.



Circle 294

MEMORY PROTECTION DEVICES

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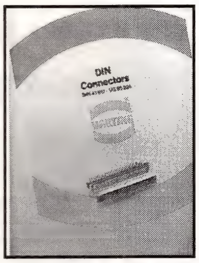

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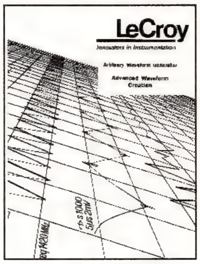
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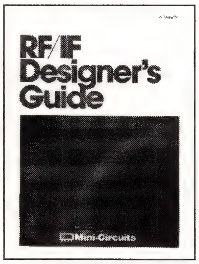

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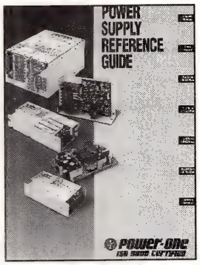
POWER-ONE POWER SUPPLIES

Power-One's new Reference Guide has over 200 standard switch-mode and linear AC to DC power supplies. Available direct from Power-One or through authorized distributors, model outputs range from 2v to 250v, up to 2,000 watts.



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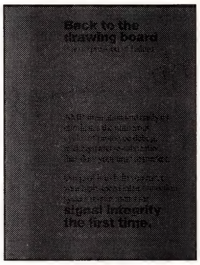

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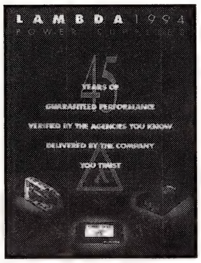
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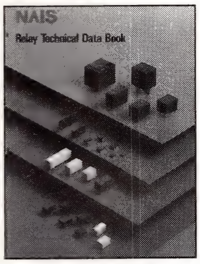

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AT&T SOLID-STATE RELAYS

The designer's Guide from AT&T Microelectronics provides design information on the LH1500 Series of low power, optically- coupled MOSFET Solid-State Relays. Details included electrical specifications, performance characteristics, outline drawings, and typical applications.

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SIMULATION SOFTWARE

AT&T Istel, Beachwood, Ohio, is offering a full-color, eight-page brochure that highlights the advantages and applications of its Witness Simulation Software. Features of Witness described include its user friendliness, easy access menus, available support services, and current compatibility with the industry's widest range of operating systems, hardware platforms, and network configurations. CM **CIRCLE 692**

HIGH-SPEED OP AMPS

A brochure from Harris Semiconductor, Melbourne, Fla., details voltage-and-current-feedback operational amplifiers, and buffers with bandwidths ranging from 45 to 850 MHz. It provides a quick and comprehensive reference to certain parts introduced since publication of Harris's 1306-page Linear & Telecom ICs for Analog Signal Processing Applications 1993-1994 databook. The free brochure, "High-Performance Op-Amps and Buffers," contains AnswerFAX instructions to instantly receive full data sheets via fax. In addition to tables of standard op-amp/buffer performance specifications, the brochure explains an array of architectural features that broaden the possibilities for device selection. These include multi-amp configurations that provide per-amplifier enable/disable for simple signal multiplexing. CM **CIRCLE 693**

HANDBOOK OF PC INSTRUMENTS

Intelligent Instrumentation, Tucson, Ariz., has released the 7th edition of its *Handbook Of Personal Computer Instrumentation*. The PCI Handbook, which is available for free, is a respected source for PC-based data acquisition, test, measurement, and control information. Topics include fundamentals of signal conditioning, wiring, shielding, and data acquisition. Also contained are techniques and practical application notes. The 228-page edition has been completely revised to reflect the latest technology. Intelligent Instrumentation's broad line of hardware and software products are described, along with system-configuration guidelines. The company manufactures data acquisition, test, measurement control, and DSP products for PC/XT/AT (ISA), EISA, Micro Channel, and Macintosh II NuBus computers. These include analog and digital I/O boards, IEEE-488 interface boards, signal conditioners, and wire-termination products. Converters in the 12- to 18-bit range with speeds up to 10 MHz are included. CM **CIRCLE 694**

INTERFACE PANELS CAPABILITIES OUTLINED

In a color brochure, Cherry Electrical Products, Waukegan, Ill., outlines its capabilities in designing electronic interface panels. These man-to-machine interfaces can make or break an end product. The brochure explains Cherry's expertise in designing and assembling interface panels that can make a difference. Sections cover customized panel design, advanced manufacturing, quality issues, and the company's worldwide resources. DM **CIRCLE 695**

SURFACE-MOUNT PASSIVES FILL 52-PAGE CATALOG

A full-line catalog of surface-mount passive components is available from Cal-Chip Electronics Inc., Warminster, Pa. Included in the 52-page catalog are multilayer ceramic chip capacitors, SMT chip resistors, multilayer chip inductors, ferrite chip beads, SMT tantalum and aluminum electrolytic capacitors, and discoidal chip capacitors. Detailed charts and graphs are included in addition to photos, features, applications, specifications, sizes, and dimensions. DM **CIRCLE 696**

LOW-NOISE MICROPHONE PREAMP

Application note AN-242, "A Low Noise Microphone Preamp with a Phantom Power Option," from Analog Devices, Wilmington, Mass., describes the design and application of a high-performance two-IC microphone preamp. A schematic diagram is included, as well as considerations for obtaining optimum sonic performance. The combined features of Analog Devices' SSM-2017 differential input audio IC and OP-275 dual bipolar/JFET low-noise op amp are shown in this circuit, used for a variable gain microphone preamp with optional phantom power. Phantom power allows users to remotely power condenser microphones, preamps, and active direct boxes on the same wires that are used to carry the audio signal. Radio frequency interference, as a potential problem for high-gain preamps, is investigated. Output control and performance are discussed. Gain and noise performance of the two-chip preamplifier are graphed. CM **CIRCLE 697**

POWER SUPPLIES, TEST SYSTEMS

The DC Power Products Catalog from Hewlett-Packard, Palo Alto, Calif., details specifications of the company's power supplies, electronic loads, and power-supply test systems. The 56-page catalog is organized to help engineers select the appropriate power supply or electronic load for each application. An applications section helps users solve common technical problems, such as remote sensing, multiple-power-supply applications, and connections for unusual configurations. Power products include HP-IB computer-controlled dc power supplies ranging from 25 W per output to 5000-W models. Single- and multiple-output models are listed along with modules configured for power-supply mainframes. Also listed are a wide assortment of manually controlled and analog-controllable power supplies. The catalog, part number 5091-6205, is free. CM **CIRCLE 698**

STREAMING TAPE DRIVES

A four-page, full-color brochure from Anritsu America, Rochelle Park, N.J., features all of the pertinent specifications and features of the DMT2820 and DMT2720 GCR streaming tape drives. Color photographs aid descriptions of the products' functions and capabilities. Features described include quad-density, tape speed, setup/maintenance, input voltage, tape length, and operation. The DMT2820 has a fast tape speed of 200 ips, which makes it ideal for use in high-speed systems. The DMT2720 has a tape speed of 100 ips, making it suitable for use in medium or low-speed systems. The brochure is free. CM **CIRCLE 699**

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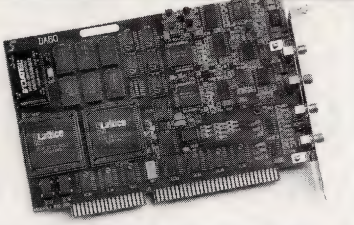

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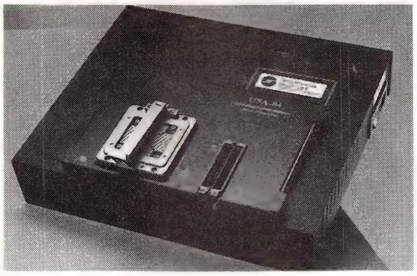

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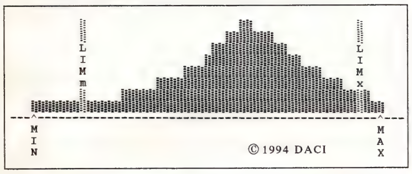

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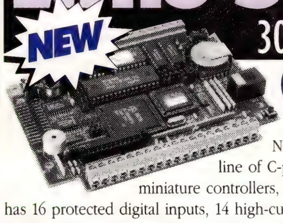

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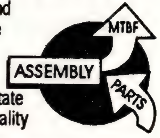

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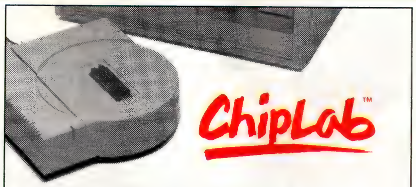

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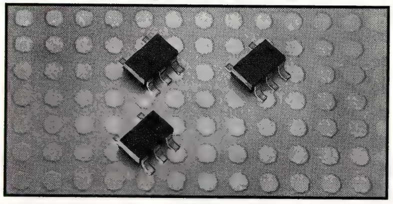

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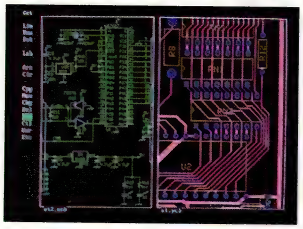

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Taipei, Taiwan R.O.C.
Phone: 011-886-2-7184407 FAX: 011-886-2-7125591
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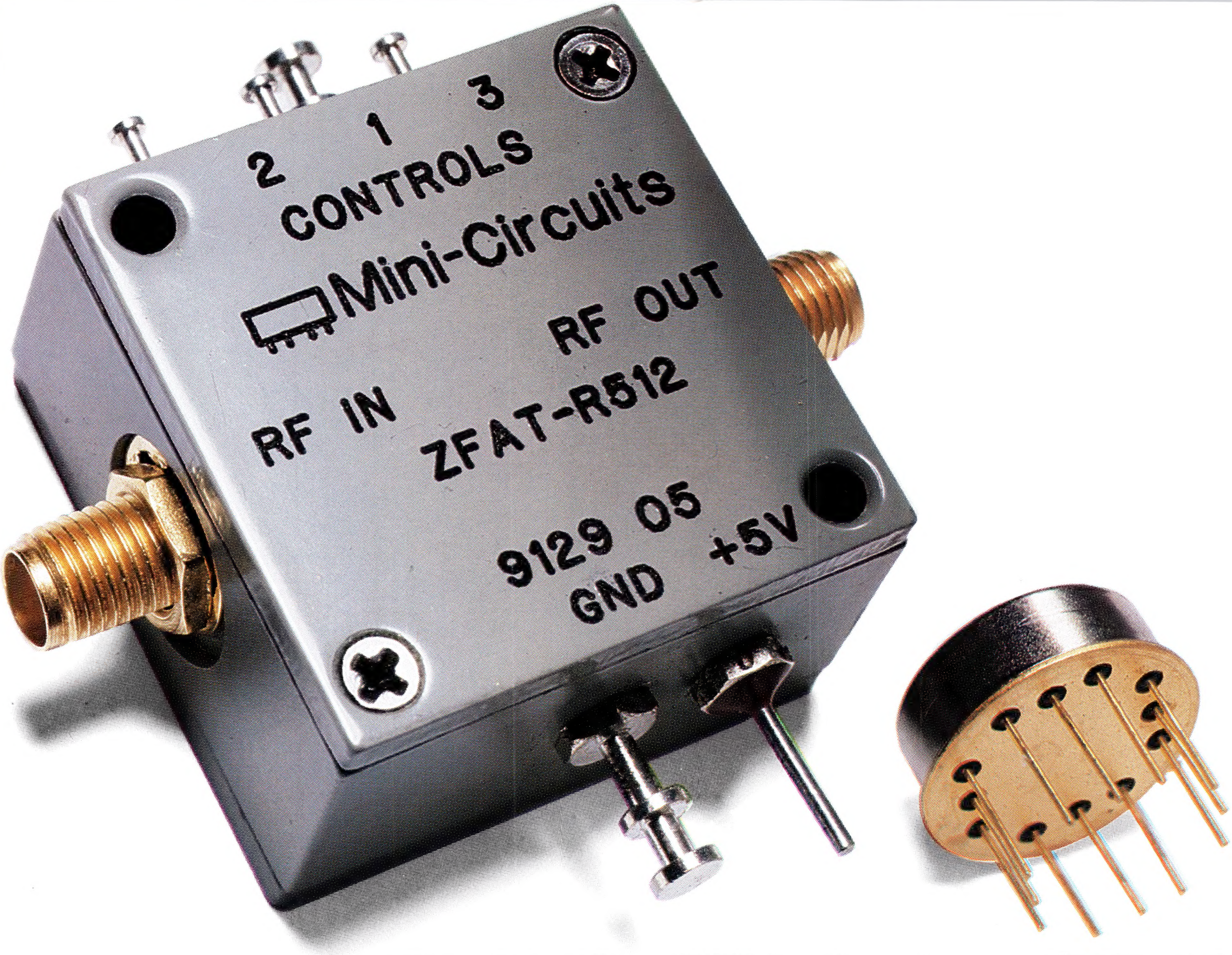

DIGITAL STEP ATTENUATORS

up to 35dB
10 to 1000MHz
FROM $5995

TOAT-R512 ZFAT-R512 Accuracy		TOAT-124 ZFAT-124 Accuracy		TOAT-3610 ZFAT-3610 Accuracy		TOAT-4816 ZFAT-4816 Accuracy		TOAT-51020 ZFAT-51020 Accuracy	
(dB)	(+/-dB)	(dB)	(+/-dB)	(dB)	(+/-dB)	(dB)	(+/-dB)	(dB)	(+/-dB)
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**4.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**8.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	12.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**16.0**	**0.5**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	20.0	0.8	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	24.0	0.8	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	28.0	1.1	35.0	1.0

Price $ (1-9 qty) TOAT $59.95/ZFAT $89.95

bold faced values are individual elements in the units

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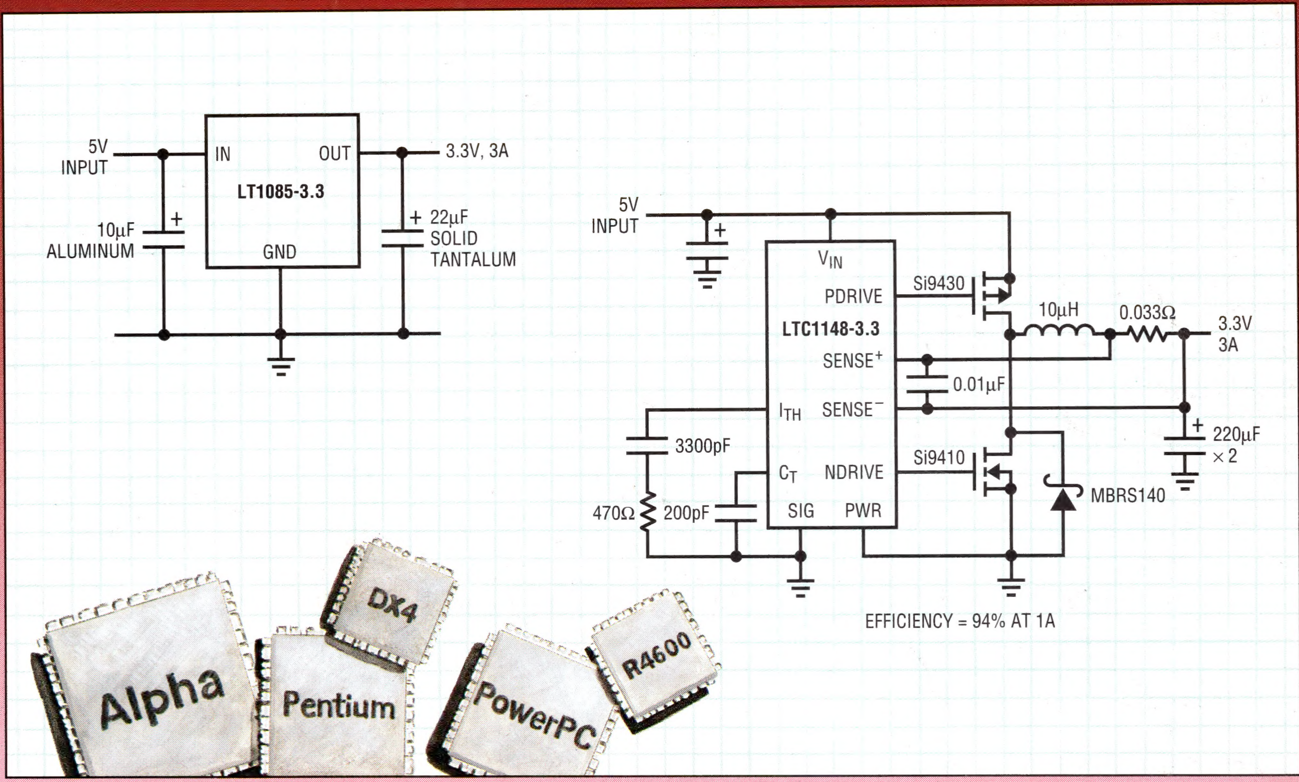
5V→3.3V: Linear or Switcher?



You have chosen your processor, now you must choose your power supply. Linear Technology provides you with the best solutions, linear regulator or switching regulator to convert from 5V to 3.3V at any current. We also allow you to tailor your output from 2.9V to 3.6V.

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Output Current	Linear Regulator	Switching Regulator
1.5A	LT1086-3.3	LTC1147-3.3
3A	LT1085-3.3	LTC1148-3.3
5A	LT1084-3.3	LTC1148-3.3
7.5A	LT1083	LTC1148-3.3
10A	LT1087 (X2)	LT1158
15A (20A Peak)	N/A	LT1158

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